A new 65nm LP metastability measurment test circuit

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Abstract— **Recent synchronizer metastability measurements indicate degradation of MTBF with technology scaling, calling for measurement and calibration circuits in 65nm and beyond. Degradation of parameters can be even worse if the system is operated at extreme supply voltages and temperature conditions. In this work we study the behavior of synchronizers in a broad range of supply voltage and temperature corners. A digital on-chip measurement system is presented that helps to characterize synchronizers in future technologies and a new calibrating system to account for supply voltage and temperature changes is shown. Measurements are compared to simulations for a fabricated 65nm bulk CMOS circuit build.**

INTRODUCTION

Multiple-clock domains System on Chip (SoC) designs require synchronization when transferring signals and data among clock domains and when receiving asynchronous inputs. Such synchronizations are often susceptible to meta-stability effects [1], which may propagate into the receiving circuit and may cause malfunctioning. To mitigate the effects associated with metastability, latches and flips flops are often used to synchronize the data [2], in schemes such as pipelined flip flops.

There is, however, a certain probability that the circuit will not resolve its metastable state correctly within the allowed time. To enable assessing the risk, and to enable the design of reliable synchronizers, models describing the failure mechanisms for latches and flip flops have been developed [1][2][3]. Most models express the risk of not resolving metastability in terms of the mean time between failures (MTBF) of the circuit (1)

$$MTBF = \frac{e^{S/\tau}}{T_W \times F_C \times F_D} \qquad (1)$$

where F_C and F_D are the clock and data frequencies, respectively, S is a pre-determined time for metastability resolution, τ is the resolution time constant, and T_W is a parameter often related to the setup-and-hold time window.

Desirable values of MTBF depend on the application and range from several years upwards. The parameter τ is predominant in synchronizer characterization since its effect on MTBF is exponential (1). Evidently, as technology scales, F_C and F_D increase and to maintain high MTBF τ must decrease as well. In the past, τ was believed to improve with technology scaling [4]. However, recent measurements [5][6] indicate that scaling trends of synchronizers should be re-considered: The need to obtain full characterization may be imperative in technologies beyond 45nm. Because of this, simulation methods that can reliably predict measurements are growing in importance. The physical testing of a system at the extremes of its operating conditions is the industry standard method for validating proper operation. For digital systems that are at risk of a metastability failure, the risk of entering metastability may be higher in extreme PVT corners. Synchronizer parameters τ and T_W in (1), can be seen as dependent on supply voltage and temperature; $\tau(V_{DD}, T), T_W(V_{DD}, T)$. As a result, careful simulation of the system design at several points throughout its operating region combined with verification is proposed as a dependable approach to the detection of potential metastability failures. This paper describes a fully digital on-chip characterization circuit to measure synchronization performance that is an improvement of the circuit shown in [7]. We show a new calibration circuit to compare measurements and simulations over a wide range of supply voltage and temperature corners for a standard library flip flop. We show good correlation between measurements and simulations. A 100x73 μm^2 on-chip digital measurement circuit was fabricated in a low power 65nm bulk CMOS process (Figure 11) and was tested to prove its utility for measurements and for validating simulation results.

1 PROPOSED CHARACTERIZATION METHOD

The measurement consists of sampling the output of the flip-flop-under-test twice: first (X in Figure 1) by the clock delayed by a factor DL (by means of a delay line) and second (Y) by the negative edge of the clock. The two samples are compared by a XOR gate Figure 1(a). A metastability event that resolves during the time window between the delayed and negative edges of the clock (namely an event that did not resolve within the allotted time DL) increments the counter (the number of events expected to resolve after the negative edge of the clock is negligible, since a low frequency clock is used). The measurement continues for time period T and thus MTBF is T divided by the counter value. The data and clock are produced by two uncorrelated sources.

The entire measurement is repeated for different DL delays, obtaining a set of (DL, MTBF) readings. This set is used to compute τ and T_W. The entire circuit of Figure 1(a) is embedded on-chip. Since this measurement procedure tests for metastability at the falling edge of the clock, it examines the recovery of only the master latch and produces τ_M (τ of master latch). If $\tau_M \neq \tau_S$, the method fails to estimate τ_S (τ of slave latch) and, consequently, may give

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erroneous values of MTBF. For each voltage it is possible to calculate MTBF as

$$MTBF = \frac{T}{\#(> DL)} \quad (2)$$

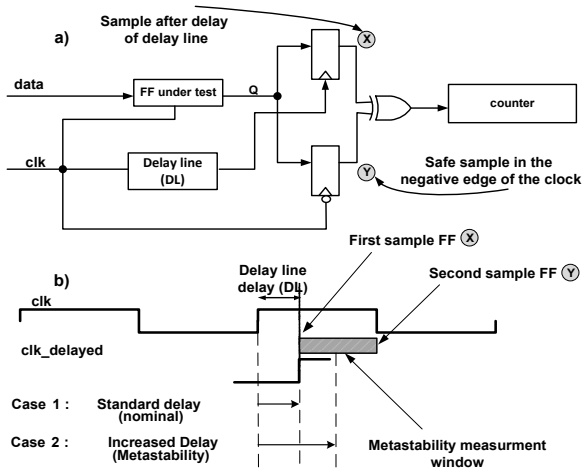

Figure 1. **(a) Metastability measurement circuit (b) Waveforms explaining the operation of measuring method.**

where #(>DL) denotes the number of resolution events that took longer than DL to resolve and T is the time period that the counter was enabled. From, (2) and *S*=DL we can derive

$$\ln(\#(> DL)) = -\frac{1}{\tau}(DL) + \ln(F_C F_D T_W T) \quad (3)$$

Thus, performing a least square fit to a linear equation of DL and ln(#(>DL)) produces a linear curve with a slope and an intercept. From (3), $\tau = -1/slope$ and $T_W = e^{y(intercept)}/F_C F_D T$.

2 Delay Line Calibration

One important step for obtaining reliable results is the delay line calibration. Both τ and T_W rely on accurate delay line values (3). A schematic of the implemented delay line is shown in Figure 2. The calibration consists of measuring the exact delay generated by the delay line in the fabricated part. For this purpose the delay line is closed into a ring oscillator (RO) and the value of the frequency generated is measured out after clock division.

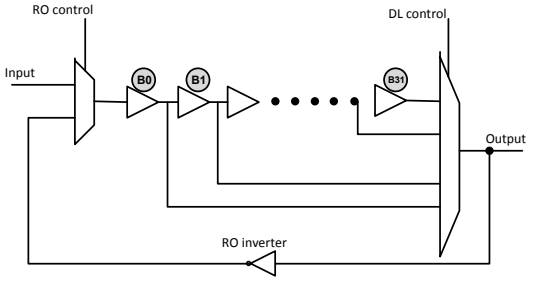

Figure 2. **Delay line circuit schematics and RO inverter.**

The period generated by the ring oscillator is given by (4), where T_{buffer} accounts for the delay of each buffer, T_{inv} is the delay of the RO inverter, T_{muxes} the delay of the two multiplexers and $T_{parastitics}$ are wiring and other parasitic delays. N is the number of buffers in the delay line, and is selected by the output multiplexer digitally.

$$T = 2\left[N \cdot T_{buffer} + T_{inv} + T_{muxes} + T_{parastitics}\right] \quad (4)$$

To obtain the exact delay between input and output, the delay of the inverter in (4) should be estimated. Since each buffer is composed of two inverters, we obtain a good estimation of T_{inv} by calculating the slope of the plot relating N and T using (4). Such a plot is shown in Figure 3.

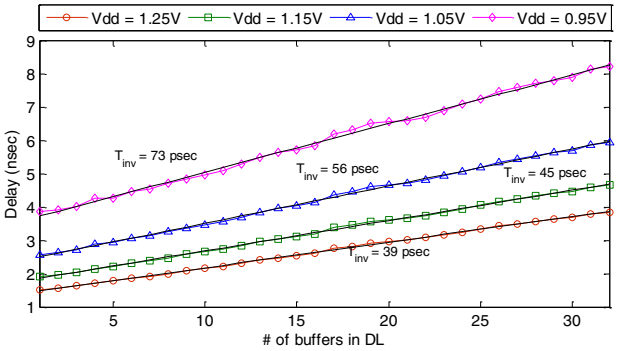

Figure 3. **Delay line delay versus number of buffers for different supply voltages at T=20C. T_{inv} estimated for each curve is shown.**

Since τ measurement is obtained from the slope in (3) and is a differential value, it is not affected by exact values of delay of the delay line. However, T_W is based on y-intercept, which is very sensitive to exact values of delay, then T_W values are more error prone than τ values. The error introduced in the exact delay measurement of the delay line (wiring delays, process variations, etc.) are estimated in the following section.

3 Results

In this section we present measurements and simulations of a library master-slave flip-flop (Figure 4), used as a synchronizer in a 65nm LP CMOS process. The measurements have been performed on a sorted TT part. Simulations used for comparison were carried out using the method described in [8], that sweeps clock and data signals to achieve accurate τ and T_W values.

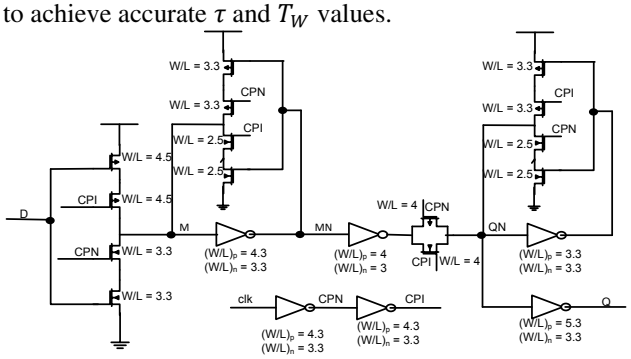

Figure 4. **Library flip-flop used for simulations and measurements.**

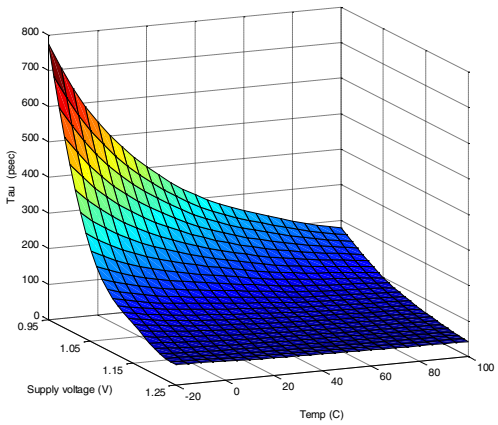

Figure 5. τ **Interpolated measurements results for different temperatures and supply voltages 3D view.**

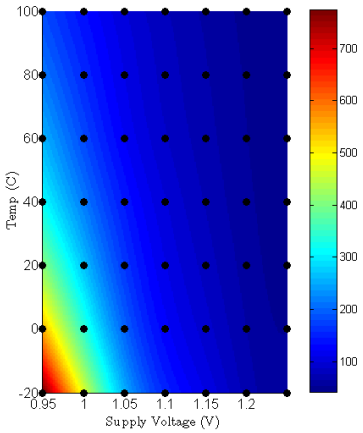

Figure 6. τ **Interpolated measurements values flat view. Actual measurement grid is marked with black circles.**

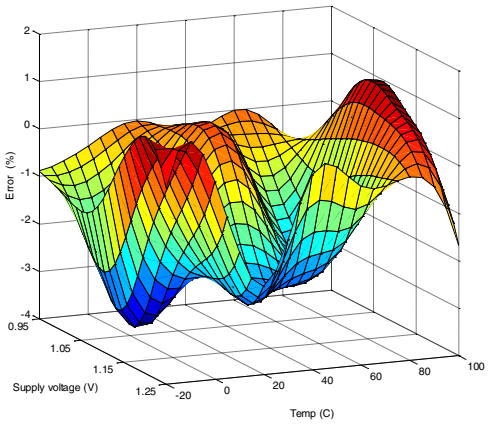

Figure 7. τ **Measurements and simulation error for different supply voltage and temperature nodes.**

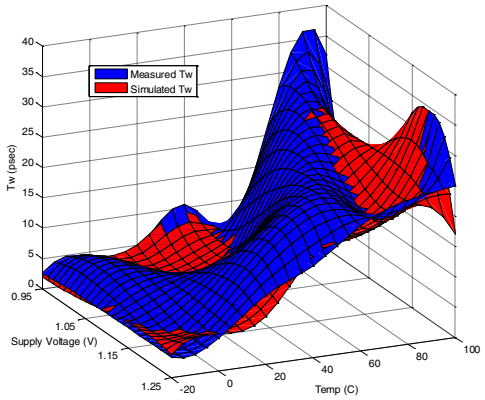

Figure 8. T_W **Interpolated measurements and simulation results for different temperatures and supply voltages 3D view.**

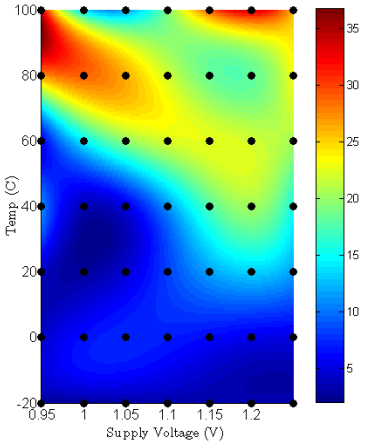

Figure 9. T_W **Interpolated measurements values flat view. Actual measurement grid is marked with black circles.**

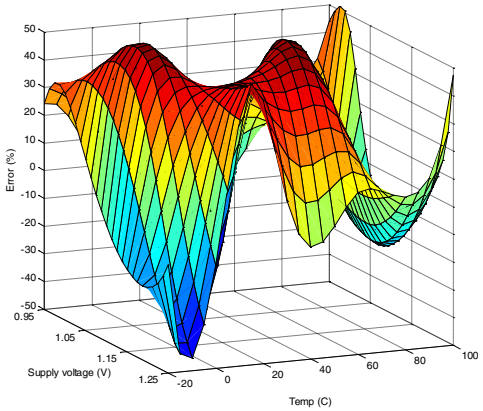

Figure 10. T_W **Measurements and simulation error for different supply voltage and temperature nodes.**

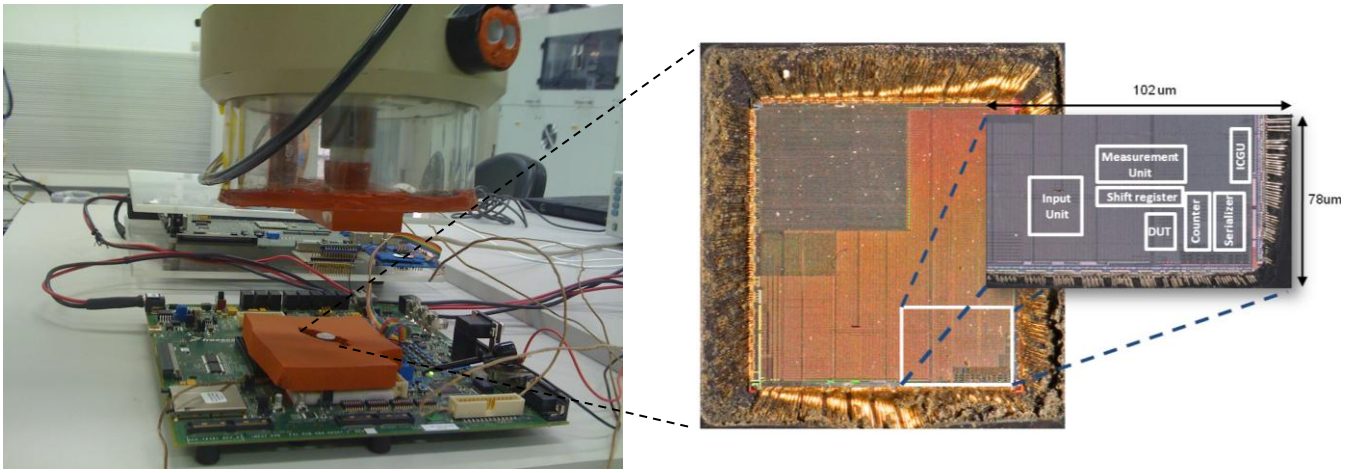

Figure 11. **(a) Board including on-chip measurement circuit with thermo stream temperature system. (b) Micrograph of the metastability measurement circuit fabricated in 65nm CMOS**

Figure 5 shows measured and simulation results for τ for different supply voltage and temperature nodes, both plots are superimposed. Actual measured and simulated nodes are marked with black dots in Figure 6, while other values are interpolated. Figure 7 shows the error in τ between measurements and simulations. The error ranges between 1.3% to -3.2% through the entire range of supply voltage and temperature nodes. For each node the delay line is calibrated and hence the deviation is due to inaccuracy in measuring DL frequency and least square error in the linear fit of (3). Those errors are most likely due to instrument precision such as oscilloscope and thermocouples for temperature measurement which are about 5%. Since the measurement is differential delay errors in delay line are compensated and the value obtained is highly accurate. **Figure 12** shows a cross section of Figure 5 for different temperature values, showing high correspondence of measurements to simulations.

Figure 8 shows T_W measured and simulated results. Figure 9 shows in black circles actual measured nodes and interpolated measured results. Figure 10 shows the error in T_W between measurements and simulations. The value of T_W is highly affected by insertion delay difference between clock to DUT and clock to delay line (Figure 1), this insertion delay is reduced to minimum in the design phase, though some parasitic still exists (part of that is accounted for by $T_{parastitics}$ in (4)). That part is not taken in account in the measurement of DL but has a high impact on the calculation of the y(intercept) in (3). Due to high process variations in deep sub-micron technologies, the delay of the RO inverter can differ highly from the mean inverter delay of the other inverters in the delay line. Those variations may reach 40% in the process used for fabricating out circuit, and that is why the value of T_W measured presents such a high variability.

The test system employs a single output pin and six input pins; in practice, such a system could be designed as fully-contained built-in test without any dedicated external pins.

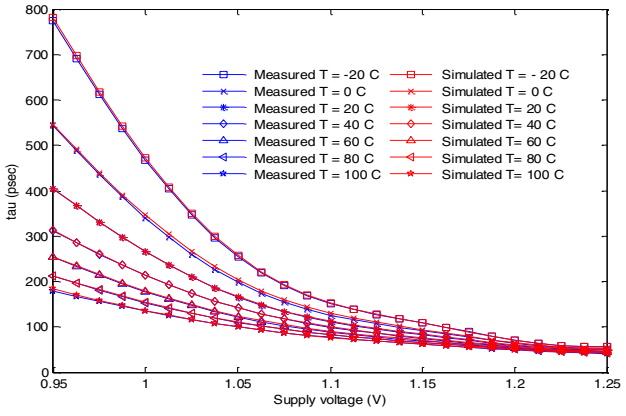

Figure 12. τ Measurements and simulation results versus supply voltage for different temperatures.

4 SUMMARY

We showed a circuit to extract synchronization parameters (τ and T_W) in a 65nm process for a wide range of supply voltages and temperatures with high efficiency. These measurements are designed to validate simulations of the parameters under varying PVT conditions. We have made measurements and simulations for a wide range of supply voltage and temperature corners and confirmed that the worst case scenario is achieved for low supply voltages and low temperatures. We compared measurements to simulations and showed that τ can be predicted with an error of less than 5%. T_W was predicted with higher variability, but its impact on MTBF is significantly smaller than that of τ.

Since the measurement circuit requires only two constant frequency sources and produces a digital output, it can be applied to a self-calibrating synchronizer design, which can be adjusted automatically and dynamically to varying circumstances such as process variations and environmental conditions (voltage and temperature), as well as to DVFS systems where voltage and clock frequencies may vary from time to time. Such self-calibration circuit may change the number of series FFs included in synchronizers in order to assure the desired level of reliability under changing conditions.

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