Radiation Characterization of a Dual Core LEON3-FT Processor

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***Abstract*—GR712RC is a dual core 32-bit fault-tolerant SPARC^{TM}V8/LEON3-FT processor that has been developed and manufactured by Ramon Chip Ltd and AeroflexGaisler AB and characterized for radiation effects. It is designed with AeroflexGaisler's intellectual property and implemented with Ramon Chip's RadSafe^{TM} radiation-hard-by-design library in a commercial 0.18µm shallow trench isolation CMOS process. Radiation test results for total ionizing dose, single event latch-up and single event upset data with correction/data-restore methodologies are reported, demonstrating its suitability for operating in a space environment.**

***Index Terms*— Single Event Upsets, Total Ionizing Dose, Processor, Error correction.**

I. Introduction

Radiation effects can be a significant problem for devices operating in a space environment. Soft errors, in particularly,is a problem for processors because of their complexity.

In a commercial 0.18µm shallow trench isolation CMOS process, Ramon Chip Ltd together with AeroflexGaisler AB has developed and manufactured a dual core version of the LEON3-FT processor with radiation tolerance to all radiation effects of concern in a space environment. Part of the radiation tolerance is achieved with Ramon Chip's RadSafe^{TM} radiation-hard-by-design library: Single Event Latch-up (SEL) immunity; Total Ionizing Dose (TID) immunity up to 300 krad(Si); Single Event Upset (SEU) hardening of sequential logic and configuration registers by means of SEU hardened flip-flops; Single Event Transient (SET) hardening of combinatorial logic, clock networks, and Delay-Locked-Loop (DLL) circuits. Remaining hardening of all on-chip SRAM memories is achieved by error correction techniques provided by AeroflexGaisler with the fault tolerant version of the LEON3 processor. The radiation hardening concept is similar,but not identical, to the one used for the UT699 LEON3-FT processor provided by Aeroflex Colorado Springs. Radiation test results of UT699 were reported in 2009 [1].

This paper reportsradiation test resultsfor TID, SEL, and SEU of the newly developed processor.It also reports on the soft error protection concept implemented in the processor. Single event upset testing is performed with application tests representing a worst-case scenario for actual application cases in a space environment.

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II. Experimental Details

A. Product Description

The tested GR712RC device is a pipelined monolithic, high-performance, fault tolerant 32-bit SPARC^{TM} V8 LEON3-FT dual core processor[2], [3]. A compliant 2.0 AMBA bus interface integrates the two on-chip LEON3-FT processor cores with a memory controller, a 192 kbyte on-chip RAM memory with EDAC, two RMAP SpaceWire ports, programmable interrupt peripherals, a timer unit with four timers including watchdog, and a switch matrix for additional interfacing of among others Ethernet, four additional SpaceWire ports, six UARTs, CCSDS TM/TC, Mil-Std-1553B, two CAN controllers, general purpose I/Os, SPI, and I2C. Fig. 1 is showing a functional block diagram of GR712RC. The GR712RC is SPARC V8 compliant; compilers and kernels for SPARC V8 can therefore be used as industry standard development tools.

The device is powered with a nominal 3.3V I/O and 1.8V core voltage. 100% load of both processors operating at 100 MHz clock frequency results in power consumption of 1.5 Watt. The device operates up to 125 MHz from -55°C to +125°C.

B. Soft ErrorProtection Concept

The LEON3-FT fault-tolerance features are designed to detect and correct SEU errors in on-chip SRAM memories. The features can be divided in two categories: cache memory protection and register file protection. The cache memory in GR712RC consists of separate instructions and data caches, each 16 kbyte large. Each cache has two parts; tags and data memory. The tag and data memories are implemented with on-chip SRAM memories and protected with four parity bits per 32-bit word, allowing detection of up to four simultaneous errors per cache word. Upon a detected error, the corresponding cache line is flushed and the instruction is restarted. This operation takes 6 clock cycles and is transparent to software.

The processor's Integer Unit (IU) register file is

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implemented with on-chip SRAM memories.It is protected using Bose-Chaudhuri-Hocquenghem (BCH) coding [4] capable of correcting one error and detecting two errors (SEC/DED) using seven check-bits per 32-bit word. The error detection and corrections has no impact on normal operation, but thecorrection will delay the current instruction by 6 clock cycles. An uncorrectable error in the IU register file will generate a register-file error-trap (thiswas never recorded in the heavy ion tests).

Error checking and correction of cache andIU register file memory is only performed during memory reads and is therefore dependent upon the application, clock speed, and memory access rates.For diagnostic purposes, error counters are provided to monitor detected and corrected errors in both the IU register file and tag and data parts of the two caches.

The register file of the Floating Point Unit (FPU) is implemented with the hardened flip-flops provided with the RadSafe^{TM} library. No additional error correction of the FPU is implemented.

The all-digital DLLs are protected from SEUs by using hardened flip-flops. The clock network is protected from SETs with dedicated glitch filters.

C. Test System

The test hardware consists of a boardhosting one GR712RC device connected to one Flash PROM device, one SRAMdevice,and one UART RS232 transceiver device. Additional circuitson the board are an oscillator providing the system clock;three power regulators on the board distributing power to the core and I/Os of the GR712RC and the peripheral circuits; and a power management circuit controlling the reset signal to the GR712RC and the memory devices.

A host computer is connected via the UART interface to the GR712RC. During irradiation,a test software is running on the GR712RC reporting its status and results to the host computer running a dedicated monitoring software.

The watchdog output of GR712RC [3] is connected to the power management circuit. In this way, any watchdog timeout event leads to an automatic reset of the GR712RC.

The test software is stored in the Flash PROM. At reset and start-up of the processor the software is transferred from the Flash PROM to the SRAM wherefrom the software is executed.

D. Test Software

Two different test programs have been used for SEU testing,: “IU-test” and “Paranoia test”. While the Device Under Test (DUT) isbeing irradiated, one of thesetest programsis executed continuously. In each loop of the test program, a self-checking test task is executed and any test failure is reported to the host computer over the UART channel. Moreover, it reports results and its status to the host: that it is actually running, the value of the internal memory error counters,and the status of the trap registers of the processor.With the continuous reporting of the internal error counters, the total number of corrected errors in the memories is derived for each test run. After reporting of a trap event the software triggers a reset of the processor by causing a watchdog timeout.

The “IU-test” is a synthetic application designed to access all caches and the IU register file. Each iteration of the test program operates in four steps: a dataarray with the size of the data cache is allocated and initialized with predefined contents (a), a checksum is calculatedby summing the contents of the array (b), the checksum is compared against a pre-calculated value (c), if the resultis not equal an“IU data error” is reported to the host system (d). Since the allocated data array (a) has the same sizeas the data cache, all locations of the data cache will be accessedin each iteration.The calculation of the checksum (b) is done with discrete statements rather than a short loop. The code size for the checksumroutine is thereby large enough to utilize the full instruction cache in each iteration. To test all registers inthe register file, a recursive routine is called once in each iteration. The recursion is 13

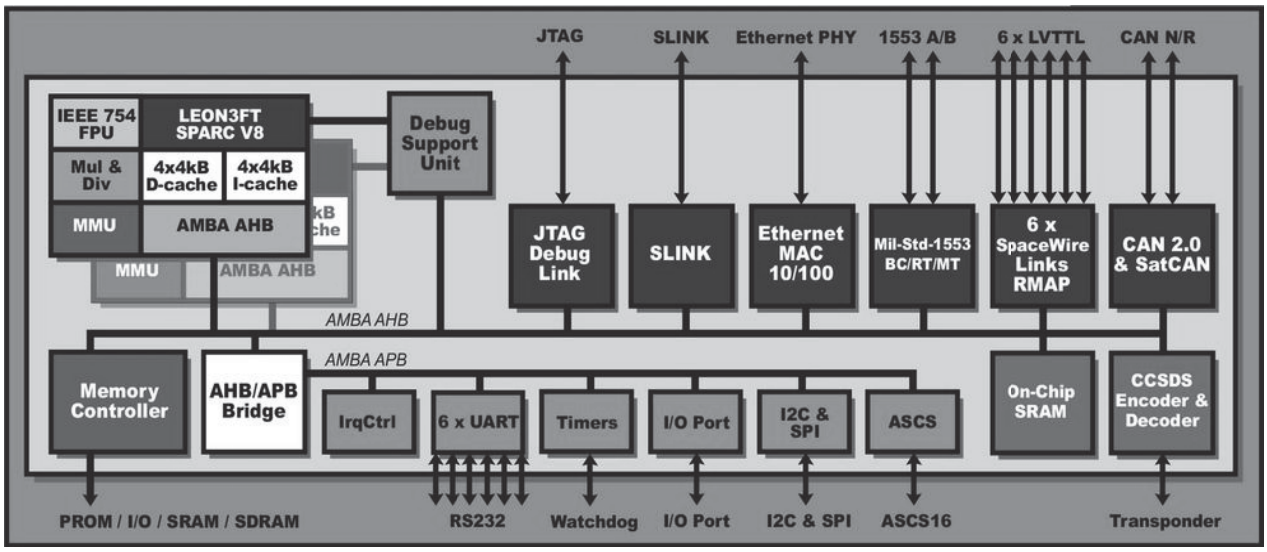

Fig. 1.All functional blocks available in GR712RC.

levels deep and guarantees that all registerwindows will be written to memory and then restored again. The "IU-test" program thus achieves near 100% coverageof all on-chip memory during each iteration of the software. Operating at 100 MHz, each iteration takes 3.6 ms. The risk for error build-up during one iteration is thus minimal.

The "Paranoia test" executes the double-precision Paranoia FPU validation test bench [5]. The test bench performs numerous tests to validate the floating-point handling of a processor. All FPU calculations are verified against values calculated in the IU. The program consists mostly of integer instructions; only 5% of the executed instructions are floating-point operations. The program is almost totally self-checking; any undetected errors in the FPU calculations would be detected as an"FPU data error"by the software cross-checking. Also undetected errors in IU can cause a reported failure as a result of the cross-checking between IU and FPU. In the same manner as in the "IU test" a recursive routine is called beforeeach iteration of the "Paranoia test". Operating at 100 MHz, each iteration takes 6.6 ms.

Both these test programs have earlier been used for SEU testing of the UT699 processor [1], but are here modified to fit the configuration of the GR712RC processor.

E. Single Event Latch-up Testing

GR712RC was tested under worst-case conditions for Single Event Latch-up (SEL), which is at maximum temperature and voltage. With heating element the DUT was heated to +125°C. The temperature was monitored with a PT100 element attached to the package body. The supply voltages were set to 3.66 V and 1.98 V for I/O and core, respectively. The SEL testing was performed with the device executing the "IU test" with a clock frequency of 10 MHz without DLL. Any event that could cause the DUT to stop operating wouldmanually be recovered by re-initiating the operation of the DUT from the host computer. The core and I/O supply current was continuously monitored for any latch-up event.

F. Single Event Upset Testing

Heavy ion SEU test of the GR712RC was performed executing the "IU test" and "Paranoia test", each in separate test runs. Three different cases for clocking and system frequency have been used:10 MHz without DLL, 100 MHz without DLL, and 100 MHz with 2xDLL enabled (50 MHz input frequency). All tests were performed at ambient temperature with supply voltages as in the SEL testing. The temperature on the package body of the device was monitored during all testing, being between +34°C and +46°C. The actual junction temperature varies with the power consumption; which is a function of the clock frequency and the running test program.

G. Total Ionizing Dose Testing

Two devices were irradiated with a Cobalt-60 source in one single irradiation step achieving a total ionizing dose of 300 krad(Si). The dose rate was 6.5 krad(Si)/h, namely longer than 46 hours of irradiation. The irradiation session was followed by 168 hours of room temperature annealing and then by 168 hours ageing at +125°C. During irradiation, annealing and ageing,the devices were static biased with nominal supply voltage. Functional test and all DC electrical parameters defined in the datasheet[3] were measured and recorded: before and after irradiation, after annealing, andafter ageing. Initial and final electrical measurements were performed at -55°C, +25°C, and +125°C whereas intermediate electrical measurements were performed at +25°C only.

TABLE I
TEST CONDITIONS FOR SINGLE EVENT LATCH-UP TESTS

Device No.	Ion	Energy MeV	Tilt	Range	Effective LET MeV-cm^2/mg	Fluence ions/cm^2
#1	Xe	420	0°	37µm	67,7	1.0x10^7
#2	Xe	420	55°	21µm	118	1.0x10^7
#2	Xe	420	55°	21µm	118	1.0x10^7
#1	Xe	420	0°	37µm	67,7	1.0x10^7

The clock frequency was 10MHz with no DLL used. No SEL was recorded.

H. Test Facilities

Heavy ion testing was performed at the Heavy Ion Irradiation Facility (HIF) of CYCLONE [6], [7] in Louvain-La-Neuve, Belgium.The M/Q=4 and the M/Q=5 cocktails were used providing LETs ranging from 1.1 MeV·cm^2/mg to 32.6 MeV·cm^2/mg and from 3.3 MeV·cm^2/mgto 67.7 MeV·cm^2/mg, respectively.

Total ionizing dose testing was performed with the Cobalt-60 source at Soreq Nuclear Research Center in Israel.

III. RESULTS

A. Total Ionizing Dose

Of all electrical parameters measured after irradiation, annealing and ageing, the only change recorded was a small increase of the standby supply current. Highest current was

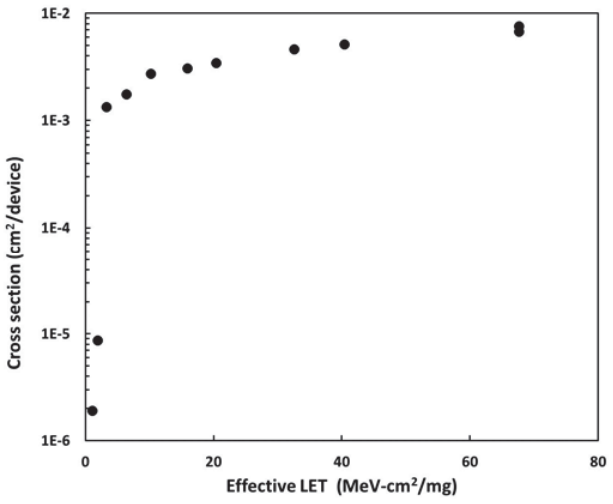

Fig. 2. Error cross section as a function of effective LET for corrected errors in the "IU test".

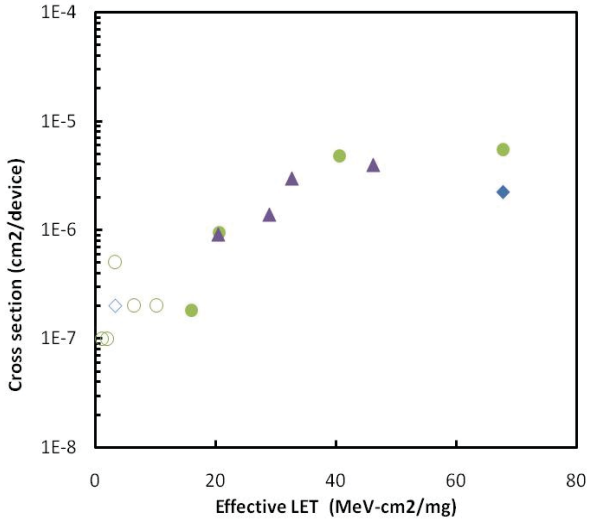

Fig. 3.Average error cross section as a function of effective LET for residual errors in the "IU test".

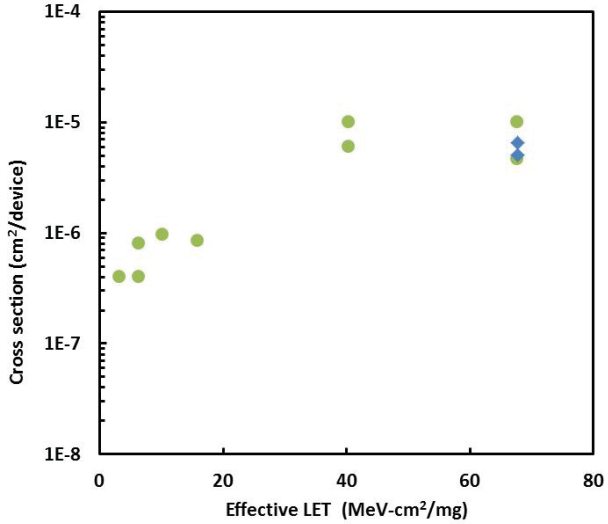

Fig. 5. Error cross section as a function of effective LET for the residual errors in the "Paranoia test".

measured directly after irradiation. After 168 hour of annealing the current returned to 46 mA,compared to the initial measurement which was below 50 µA.After ageing the current returned to the initial value.

B. Heavy Ion Testing

SEL testing up to a fluence of $1 \cdot 10^7$ ions/cm^2 was performed on two devices at highest available LET without recording any latch-up. Tests were performed with normal incident angle and 55° tilting, achieving an effective LET of 67.7 MeV·cm^2/mgand 118 MeV·cm^2/mg, respectively. All tests are summarized in Table I.

SEU testing was performed with the "IU test" and "Paranoia test". Results of corrected errors in "IU test" performed at 100 MHz without DLL are presented in Fig. 2. Each test run presented in Fig. 2 was ended after achieving at least 500 detected errors or a total fluence of $1 \cdot 10^7$ ions/cm^2. The flux was kept low ensuring correct error counting, in all test runs the average error rate was below 0.1 errors per test iteration.

All errors reported in Fig. 2 were corrected and handled by the built-in fault-tolerance of the processor; no "IU data error" was recorded. Still some residual errors,not directly related to the test task of the "IU test" itself, have been recorded.In Fig. 3, all residual errors with the "IU test" are reported. The data are presented per the different cases of clocking: 100 MHz without DLL in filled circles, 10 MHz without DLL in filled squares and 100 MHz with 2xDLL in filled triangles. Open markers represents tests where no residual errors were recorded, visualized with the reciprocal of the total fluence of these test runs. Statistics are very low, each data point represents the average value over several test runs at each LET, still only achieving between one and six errors per data point.

In Fig. 4 all residual errors in test runs with 100 MHz without DLL are reported per error type: at "IU data error" an error was reported by the "IU test"software; at "Link lost" the

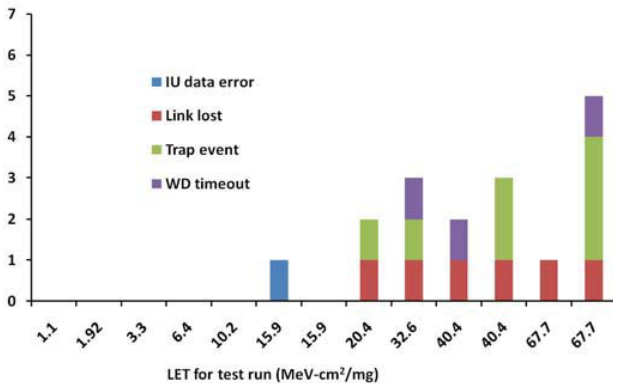

Fig. 4.Number of residual errors per test run in "IU test", classified per error type. Data from test runs with 100MHz without DLL is presented.

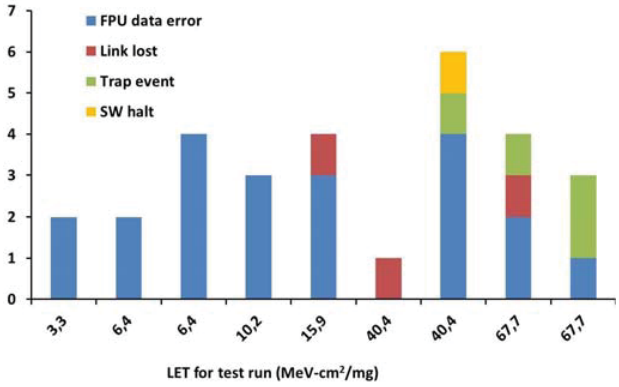

Fig. 6.Number of residual errors per test run in "Paranoia test", classified per error type. Data from test runs with 100MHz without DLL is presented.

communication between host computer and the DUT was lost; at "Trap event" the test program detected an processor trap event and recovered itself by triggering the watchdog circuit; at "WD timeout" a timeout condition triggered the watchdog circuit and at "SW halt" the test program halted and was restarted by the host computer automatically.The "IU data error" at a LET of 15.9 MeV·cm^2/mg presented in Fig. 4 was recorded in a test run with very high flux ($1{\cdot}10^4$ ions/cm^2/s) in order to achieve high fluence($5{\cdot}10^6$ ions/cm^2) within reasonable test time.

In total over all test runs with "IU test", 98,531 errors have been detected, corrected and handled by the built-in fault-tolerance of the processor. Only 28 residual errors have been recorded, all at an LET of 15.9 MeV·cm^2/mg and above. Of the residual error types (Fig. 4), no preference of error type can be distinguished.

In Fig. 5, residual errors with the "Paranoia test" are reported per the different cases of clocking: 100 MHz without DLL in circles and 10 MHz without DLL in squares. In total over all test runs with "Paranoia test", 14,362 have been detected, corrected and handled by the built-in fault-tolerance of the processor. Only 40 residual errors have been recorded. In Fig. 6 residual errors in test runs with 100 MHz without DLL are reported per error type. The "FPU data error" is dominating in the "Paranoia test",especially at an LET of 15.9 MeV·cm^2/mg and below.

IV. Discussions

A. Total Ionizing Dose

The TID test demonstrates that the device is capable for 300 krad(Si) space environment. The increase of the standby current is marginal and no other electrical parameters have been affected. The recovery of the standby current after ageing demonstrates that no rebound effects exist. Thereby, it can be concluded, in accordance with MIL-STD-883 test method 1019 [8], that the measurement of 46 mA after 168 hour of annealing represent the worst case standby current increase in a space environment of 300 krad(Si) where the dose rate is many order of magnitudes lower than the one used in the TID test.

B. Single Event Upset characteristics of SRAM elements

The error statics gathered in heavy ion test in Fig.2 can be correlated to the actual upset cross section of the underlying SRAM elements by comparing the results with simulated SEU testing by means error injection. While running the test programs under same conditions as in heavy ion test, errors was randomly injected into the cache data and IU register file via the debug interface of the GR712RC using the GRMON [10].The error counting of the test program ("Effective Errors") is compared to the statistics of injected errors in Table IIfor the "IU test".

TABLE II
Results of Error Injection with "IU test"

Module	Injected Errors	Effective Errors	Ratio Effective/Injected
Instruction cache tags	1,187	1,171	98.7%
Instruction cache data	8,432	4,287	50.8%
Data cache tags	2,263	2,238	98.9%
Data cache data	8,784	7,072	80.5%
IU Register File	638	208	32.6%
Total	***21,522***	***14,976***	***69.6%***

System frequency was 100 MHz with in average 0.5 errors per second injected randomly for twelve hours.

The SRAM bit cross section can be estimated by dividing measured error cross section in heavy ion test with the detection ratio determined with error injection and dividing with the total number of bits. For the "IU test", the detection ratio is 69.7%. The total number of SRAM bits, including check bits, in the cache memoires and IU register file is 432,128. Hence the measured saturation cross section of the "IU test" of $6.6{\cdot}10^{-3}$ cm^2/device (Fig. 2) corresponds to a SRAM bit saturation cross section $1.6{\cdot}10^{-8}$ cm^2/bit. The result correlates well with earlier SEU test data on SRAM test structures performed on a test chip for the RadSafe^{TM} library [9], especially at lower LETs. At higher LETs the measured cross section on the test structures is three times higher. This could be an effect of different supply voltages (1.8 V/3.3 V versus 1.98 V / 3.66 V);the SEU sensitivity in CMOS is known to decrease with increasing supply voltage. Moreover, it couldbe an effect of multi bit upsets from single ion strikes at higher LETs. The error counters for the cache in GR712RC can report up to four bit errors within one word as a single error. Thus, error counting including any multi bit error is underestimating the true number of upsets, although the errors have been corrected. However, this is not likely to be the case, since no double bit errorswithin in a word have been reported from the error correction of the register file. Apparently, the memories have been effectively scrambled and thereby overrun the possibility for multi bit upsets within a word.

The results of the "IU test" have demonstrated the effectiveness to correct all errors from single ion strikes with no error build-up jeopardizing the error protection. In theory, multi ion strikes in one word before any previous errors in the same word have been corrected could jeopardize the error protections. However, the probability for this to occur in a space environment is negligible thanks to the low flux and continuously accessing of the cache and register file achievedwith normal usage of the processor. The actual probability for multi bit errors can be calculated: with SRAM SEU cross sectiondata presented in this work, the intended orbit of the spacecraft, andthe maximumtime(t_{acc}) between accesses of cache and register file for the specific application case.

In [1] a simplified and conservativeequation, derived from the binomial distribution, for predicting the multi bit error rate (MBE_{rate}) is proposed:

$$MBE_{rate} = \frac{{SEU_{rate}}^2 \cdot t_{acc}}{N} \quad (1)$$

where;SEU_{rate} is the predicted SEU rate in orbit before

TABLE III
PREDICTED MULTI BIT ERROR RATE IN A GEOSYNCHRONOUS ORBIT

SEU_{rate} errors/device/s	t_{acc}	Number of words (N)	MBE_{rate} errors/device/day
$5.8 \cdot 10^{-7}$	500ms	34,816	$4 \cdot 10^{-13}$

correction in per device and seconds;t_{acc} is in seconds; and N is the number of words in the register file and cache.Note that equation (1) is only valid when $SEU_{rate} << t_{acc}$.

In Table III the SEU rate is presented for a geosynchronous orbit with the predicted multi bit error rate,using equation in (1), foran application case where t_{acc} = 500 ms.All words in register file (2 kb) and cache (2x16 kb)are assumed to be used.The SEU rate was calculated with the same model and input parameters as in section III-E below,using the SEU data presented in Fig. 2. The SEU datawas divided with the ratio between effective and injected error in Table II in order to estimate the SEU rate for the full memory content.This MBE_{rate}calculation is conservative since it assumes all multi bit upsets in a word will cause an error while the cache memories are capable of correcting up to four bit errors per word. Moreover, error injection simulation in Table II demonstrates that not all injected errors can become effective. Even with this conservatism, the calculation confirms that the probability for errors from multi bit upsets in a typical space environment is negligible.

C. Residual Errors in Single Event Upset tests

The SEU tests have demonstrated that GR712RC is very effective in correcting upsets in the SRAM elements. In total over all test runs, 112,893 upset in SRAM elements have been corrected and handled by the built-in fault-tolerance of the processor. Residual errors presented in Fig. 4 and Fig. 6represent a small portion of all errors. In total, only 68residual errors have been recorded. It must be noticed that in order to achieve interpretable results, extraordinary high fluence was used.

Theresidual errors can either have been caused by upsets in SRAM elementsthat could not be handled by built-in fault tolerance of the processor; or upsets in sequential logic and configuration registers which only are protected by means of the radiation hardening of the RadSafe^{TM} library itself. In fact, the onset LET of residual errors in "IU test" (Fig. 3) correlates quite well with the SEU data on radiation hardened flip-flops, previously tested on a test chip [9]. Hence, although test statistics is limited, it is reasonable to assume that none of the residual errors in the "IU test" have been caused by upsets in SRAM elementsbut by upsets in otherlogic protected by the RadSafe^{TM} library itself, like the flip-flops. An assumption that is further supported by the fact that no residual errors have been recorded in error injection simulations with the "IU test" (Table II).

TABLE IV
ERROR STATISTICS FOR "FPU DATA ERROR" AND FPU EXCEPTION TRAP IN "PARANOIA TEST"

Test run	LET MeV·cm^2/mg	Data Error	Trap	Corrected Errors	Ratio
#11	3.3	2	0	1549	0.13%
#14	6.4	2	0	2191	0.09%
#15	6.4	4	0	2177	0.18%
#40	10.2	3	0	1903	0.16%
#17	15.9	3	0	2326	0.13%
#20	40.4	0	0	195	0.00%
#21	40.4	4	0	573	0.70%
#8	67.7	2	*0*	312	0.64%
#9	67.7	1	1	860	0.23%
#3	67.7	1	*0*	294	0.34%
#4	67.7	5	*0*	1982	0.25%
Total	***All***	***27***	***1***	***14362***	***0.19%***

The clock frequency was 10 MHz for test run #3 and #4 and 100 MHz for all other runs. The DLL was not used.

Residual errors in the "Paranoia test" are dominated by "FPU data errors". Below the onset LET for residual errors in the "IU test", 15 MeV·cm^2/mg, the "FPU data error" is the only recorded error type (Fig. 6). Thus it can be assumed that the "FPU data errors"are residual errors in SRAM elementsnot detected or correctly handled by the built-in fault tolerance of the processor. After completion of the heavy ion test, thorough error injection simulations have been performed with the "Paranoia test". The time of injection have been extended in order to inject a large amount of errors, far more than what is expected in a space environment. Thesesimulations have revealed that a very small portion of all injected errors,instead of being correctly handled,caused either a "FPU data error" or an FPU exception trap (tt=0x08, [2]). It appears that erroneous data are feed into the FPU which either cause; a mismatch in FPU data and IU data within the Paranoia test being reported as a "FPU data error"; or a non-allowed FPU operation due to erroneous data, like e.g. division by zero, reported as an FPU exception trap. In Table IV, the ratio between these two errors and the corrected errors is presented per test run. Considering the statistical variations it can be concluded that the ratio correlates well with the ratio of 0.2% determined in error injection simulation.

Additional error injection simulation has been performed with a real-world application software, running an altitude control algorithm. The same software, named "GTB", has earlier been used in heavy ion tests [1].This software is more FPU intense; 15% FPU instructions versus 5% for the "Paranoia test". In error injection simulations, in total 420,605 errors were corrected resulting in no output errors.Thus the ratio between data errors and corrected errors was below 0.00024%, namely nearthree orders of magnitudes lower than the "Paranoia test".Apparently, the data errors in the FPU revealed with the "Paranoia test" has no correlation to the amount of FPU instructions. It may even be that not all applicationsusing the FPU need to be affected.

As a consequence of these results, an internal investigation has been launched in order to localize the problem and to define better guidelines for minimizing the probability for data errors in usage of the FPU.

D. Influence from Test Conditions

Most testing has been performed at 100 MHz which is the rated frequency of the processor. The error cross section can

be expected to decrease at lower frequencies thanks to the lower probability of latching in transients into storage elements. Little data have been collected with 10 MHz clock frequency but data in Fig. 3 and Fig. 5 give the impression that the error cross section is slightly lower with lower frequency.

DLLs (and PLLs) are circuits that can be vulnerable to single event effects. If this is the case, it would be expected that the overall error cross section increases when the DLL is active.In Fig 3, the cross section with and without DLL correlates well to each other. Thus it is concluded that the radiation hardening of the DLL provided in the RadSafe™ library and used in the GR712RC is effective.

E. ErrorRate Predictions

In paragraph III-B it has been demonstrated that the error rate as a consequence of multi upsets in the cache and IU register file for an example application case is negligible. Left to consider is the errorrate of residual errors. In Table V, predicted errorrates in a geosynchronous orbit are presented for the "Paranoia test" and the "IU test". The predictions have been performed with the CREME 96 model [11] at solar quite condition behind 100 mil of Aluminum shielding. The sensitive depth was assumed to be 0.35 µm with an additional funneling depth of1 µm.The number of bits used in the predictions has been estimated by dividing the saturation error cross sections in Fig. 3 and Fig. 5 with the measured saturation upsetcross section of the radiation hardened flip-flops, previously tested on a test chip [9].

The "Paranoia test" and "IU test" represent two worst case scenarios for an FPU intensive application and IU intensive application, respectively. In most real applications the utilization factor of the processor is lower which will reduce the actual errorrate. On the other hand, usage of both processors and peripheral cores could increase the overall error rate, but marginal; in a dual core application the utilization factor of each processor is reduced versus a single core application and the peripheral cores are smaller in area than each processor core. The criticality of different error types have not been assessed in this work. It is very application specific and must be assessed per application. Most of the error types recorded can be mitigated by means of software like e.g. exceptions trap handlingand by using the watchdog feature provided in GR712RC.

The LET threshold for the "IU test" is above 15 MeV·cm^2/mg. Thus it cannot be expected to be sensitive to proton induced upsets which implies that the errorrate in more proton rich environments but better shielded to Galactic Cosmic Rays, like low earth orbits, will be lower. For the "Paranoia test" it is the reverse, the LET threshold is low enough to expect it to be sensitive to proton upsets. Thus the errorrate may be higher in proton rich environments. However, the detection ratio of FPU data errors with the "Paranoia test"can be many orders of magnitudes higher than a real-world application using the FPU. The error rate for most applications can thus come downto the same low level as the "IU test".

TABLE V
PREDICTED ERROR RATES IN A GEOSYNCHRONOUS ORBIT PER APPLICATION TEST

Application test	No. of bits	Errors/ day	Errors/ year	Years between Errors
"Paranoia test"	210	$7.3\cdot10^{-6}$	2.7×10^{-3}	375
"IU test"	104	$2.9\cdot10^{-7}$	1.0×10^{-4}	9,407

The errorrate figures in Table IVfor a geosynchronous orbit are provided for the purpose of benchmarking against other processors, like e.g. Atmel AT697 and Aeroflex UT699. The actual errorrate must be predicted specific for each space mission.

V. CONCLUSION

Results from TID test and SEL test demonstrates the suitability for operating GR712RC in a space environment.

SEU testing demonstrates a very low error rate. Results from two application tests have been presented that represents worst casescenarios; in most real applications the utilization factor of the processor is lower which will improve the error rate figures even further.

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