A Model for Supply Voltage and Temperature Variation Effects on Synchronizer Performance

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***Abstract*— Synchronizers play a key role in multiclock domains systems on chip and their performance is usually measured by the mean-time between failures (MTBF) of the system. Recent synchronizer metastability measurements indicate degradation of MTBF with technology scaling for library flip-flop circuits in 65 nm and below. This degradation of parameters becomes critical when the system is operated under extreme supply voltage and temperature conditions. In this paper, we study the behavior of synchronizers in a broad range of supply voltage and temperature conditions. A new model for the metastability time constant (τ), the metastability window (T_W), and MTBF is presented. We show a detailed comparison of model, measurements, and simulations for different technology nodes and discuss implications for modern synchronization systems. We propose design guidelines that account for supply voltage and temperature variations and determine the correct number of synchronizer stages required for target MTBF.**

***Index Terms*— Measurement method, mean-time between failures (MTBF), metastability, resolution time constant, supply voltage dependence, synchronization, synchronizer, temperature dependence.**

I. Introduction

MULTIPLE-CLOCK system-on-chip (SoC) designs require synchronization when transferring signals and data among different clock domains and when receiving asynchronous inputs. Such synchronizations are susceptible to metastability effects [1], which may cause malfunction. To mitigate the effects associated with metastability, latches and flip-flops are often used to synchronize the data [2]. However, there is still a certain probability that the circuit will not resolve its metastable state correctly within the allowed time. To enable assessing the risk, and to design reliable synchronizers, models describing the failure mechanisms for latches and flip-flops have been developed [1]–[3]. Most models express the risk of not resolving metastability in terms of the mean-time between failures (MTBF) of the circuit

$$\text{MTBF} = \frac{e^{s/\tau}}{T_W \times F_C \times F_D} \tag{1}$$

where F_C and F_D are, respectively, the clock and data transition frequencies, S is the time allowed for metastability resolution, τ is the resolution time constant, and T_W is the parameter describing a vulnerable time window which is determined experimentally. T_W and τ are, respectively, device and technology dependents.

Desirable values of MTBF depend on the application and range from several years upward. Usually, the synchronizer design phase involves determining the number of stages that would lead to a specified MTBF for a given technology, circuit library, and operating conditions.

Note that we are assuming that the flip-flops used in the synchronizer are obtained from a predefined library. If a custom synchronizer cell can be added to the library, then much larger MTBFs can be obtained for a given number of synchronizer stages.

Recent measurements and simulations [4]–[6], [8], indicate that supply voltage and temperature variations highly affect metastability parameters, raising the need for full characterization at different operating conditions. For digital systems that are at risk of metastability failures, the risk of metastability failures may be higher in extreme PVT corners. Synchronizer parameters τ and T_W in (1) can be seen as depending on supply voltage and temperature: $\tau(V_{\text{DD}}, T)$, $T_W(V_{\text{DD}}, T)$. As a result, careful simulation of the system design at several points throughout its operating region, combined with verification, is proposed as a dependable approach to the detection of potential metastability failures. However, to discern the contribution of each parameter, we seek a formula that calculates MTBF for arbitrary combinations of V_{DD}, T, and is based on semiempirical parameters determined by measurements or simulations.

In this paper, we introduce an analytical model that is able to predict τ, T_W and MTBF with high accuracy. We provide a thorough study of the effect of supply voltage and temperature variations, and present an overall analysis, showing measurements, simulations, and model.

This paper is organized as follows. In Section II, we review previous published work on temperature and supply voltage influence on metastability parameters. A model describing τ, T_W, and MTBF under temperature and supply voltage variations is presented in Section III. Section IV shows the model results and comparisons with measurements and simulations. Section V presents different bounds for T_W and discusses synchronizer design considerations and common errors in calculating the number of synchronizer stages. Section VI summarizes the work.

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TABLE I
SUMMARY OF EXISTING METASTABILITY MEASUREMENT/SIMULATIONS RESULTS

CATEGORY	EXISTING WORK
Metastability measurements	[11],[12] – First metastability measurements, nominal V_{dd} and T. [13] –Non-constant τ measurement, nominal V_{dd} and T. [14], [15], [19], [22], [23]– Various circuits measurements, nominal V_{dd} and T. [17] – 2μm and 1,2 μm technology nodes measurements for different V_{dd} nominal T. [16] – 1.5 μm and 1.0 μm for different V_{dd}, T. [3]– 0.25 μm CMOS, nominal V_{dd} and T. [18], [20] – Programmable logic device (PLD), nominal V_{dd} and T. [6], [8],[9],[26]– 90nm CMOS FPGA, different V_{dd} nominal T [10] –Different FFs in 65nmCMOS, nominal V_{dd} and T. [27] – 40nm CMOS, nominal V_{dd} and T.
Metastability Simulations	[7] –0.35μm, 0.25 μm and 0.18 μm technology nodes, nominal V_{dd} and T. [21] – 0.18 μm CMOS, different V_{dd} and T. [24] – 65nm CMOS for different FF's and V_{dd}, nominal T. [25] –90nm[a] CMOS, different V_{dd} and body bias, nominal T.
Measurements vs. simulations	[5] – 0.18 μm[b] for different V_{dd}, nominal T. [4] – 0.65 μm[b] for different V_{dd}, nominal T.

[a] On-chip measurement method
[b] Process variability study

II. RELATED WORK

The dependence of metastability parameters on temperature and supply voltage has been studied in the literature by means of simulations and measurements. Table I summarizes relevant work in metastability measurements and simulation results under varying V_{DD}, T, and process technology. The first part of the table considers reported metastability measurements, which are performed using a wide range of methods, devices (off the shelf components, SoCs, FPGA, etc.) and diverse technology nodes. The *simulations* data in Table I represents simulation only results, without measurements to validate dependence on variations. The *measurements versus simulations* data includes publications comparing simulations with measurements for actual circuits. Rows in the table indicate different process technology or circuit.

Most publications provide measurements or simulations for a specific circuit under nominal supply voltage and temperature conditions. In [5], a comparison of simulations and measurements for varying supply voltage and temperature is performed. The publications listed in Table I shed light on the dependence of metastability parameters on supply voltage and temperature, whereas this paper combines a theoretical analysis with an exhaustive comparison between simulations and measurements over the entire relevant range. To the best of our knowledge, such model and analysis has not been proposed yet.

III. MODEL

To quantify the effect of temperature and supply voltage variations on τ, T_W, and MTBF, we seek a semiempirical formula that is able to provide insights of the physical effects influencing τ, T_W, and MTBF, while also being sufficiently simple to alleviate the need for numerous simulations at different (T, V_{dd}) combinations. For that purpose, we base our models on first-order physical effects with parameters that allow for certain degrees of freedom. Those parameters are subsequently learned using simulations or measurements.

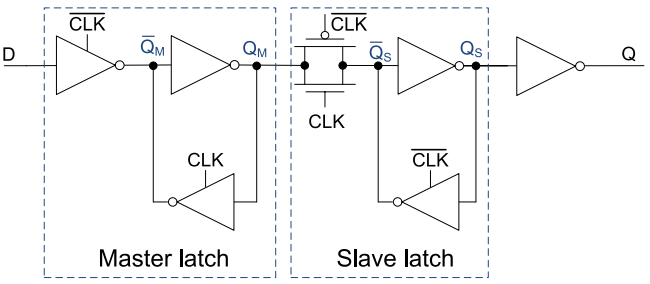

Fig. 1. Master–slave circuit.

We consider a generalized flip-flop circuit, similar to the one shown in Fig. 1. The circuit comprises a master and a slave latch. Each latch is characterized by a resolution time constant $\tau_i (i \epsilon \{m, s\})$. We start our analysis presenting a semiempirical model for τ_i, and continue to develop an empirical model for T_W. We then combine the models for τ and T_W using (1) to derive a semiempirical model for MTBF.

It is worth to note that this specific circuit topology is used as it represents a common implementation of flip-flops in digital designs and then is usually used in synchronization pipelines. However, using other topologies suited for metastability [3], [35] will result in better scaling properties as described in [44]. The model developed in this paper concerning variations in supply voltage and temperature is not constrained to any specific flip-flop circuit topology.

A. τ Model

On the basis of the resolution time constant for each latch in a flip-flop, the overall effective resolution time constant for the flip-flop is given by [28]

$$\tau_{\mathrm{eff}} = \left(\frac{\delta}{\tau_M} + \frac{(1-\delta)}{\tau_S} \right)^{-1} \tag{2}$$

where δ is the duty cycle of the clock. Using this formula, a model for the resolution time constant of each latch can be obtained and then joined using (2).

With small signal analysis, τ can be approximated by [13]

$$\tau \propto \frac{C_Q}{g_m} \tag{3}$$

where C_Q includes the gate and diffusion capacitance of the metastable synchronizer nodes $(Q_i, \bar{Q}_i, i \epsilon (m, s))$ and the coupling capacitance between the gate and the source and drain of the transistors connected to the metastable nodes. g_m is the transconductance of the transistors in the latch. In the general case of nonsymmetric latch, $\tau \propto ((C_Q / g_{m,Q})(C_{\bar{Q}} / g_{m,Q}))^{1/2}$, the geometric mean of the capacitance-transconductance ratio for each node of the latch. For the purpose of supply voltage and temperature modeling, using (3) followed by adaptation to simulated values will be

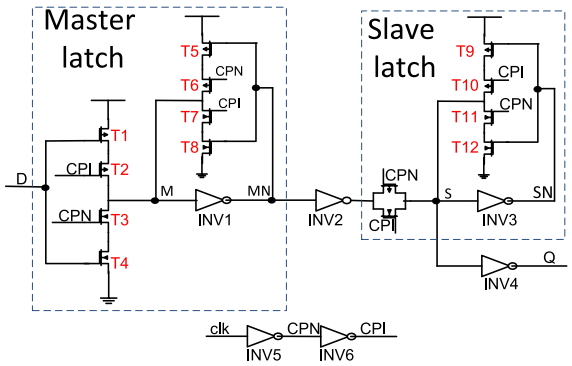

Fig. 2. Library flip-flop circuit.

shown to be a dependable approach. Fig. 2 shows a standard library flip-flop circuit. The master and slave latches are marked by dashed lines. For the master latch, C_Q includes the gate capacitances of inverter INV1, T5, T8, and INV2 and the diffusion capacitances of transistors T6, T7, T2, T3, and INV1. For g_m of the master, the transistors involved in the transconductance are T5, T6, T7, T8, and INV1.

Near metastability, the transistors operate in the saturation region, and hence the transconductance can be approximated by

$$g_m = g_{mn} + g_{mp} \propto \left(\mu_n C_{\text{ox}} \frac{W_n}{L} \frac{1}{1+\sqrt{a}} + \mu_p C_{\text{ox}} \frac{W_p}{L} \frac{\sqrt{a}}{1+\sqrt{a}}\right) \times (V_{\text{DD}} - |V_{\text{Thp}}| - V_{\text{Thp}})^{\alpha} \quad (4)$$

where $a = \mu_n W_n / \mu_p W_p$, V_{TN} and V_{TP} are, respectively, the transistor threshold voltage for the N and P transistors, respectively, μ_n and μ_p are, respectively, the electron and hole mobilities, and α is the velocity saturation index, whose typical value is around 1.3 [29]–[31].

The mobility dependence on temperature can be approximated by [32], [33]

$$\mu = \mu_0 \left(\frac{T_0}{T}\right)^{\alpha_\mu} \quad (5)$$

where T is the temperature, T_0 is the nominal temperature, μ_0 is the mobility at T_0, and α_μ is an empirical parameter referred to as the mobility temperature exponent, usually around 1.5. In a similar way, the threshold voltage dependence is given by

$$V_{\text{th}}(T) = V_{\text{Tho}} + \alpha_{\text{VTh}}(T - T_0) \quad (6)$$

where V_{Th0} is the threshold voltage at T_0 and α_{VTh} is the threshold voltage temperature coefficient, a negative coefficient with typical values around -2 mV/K [33]. Note that the *drain-induced-barrier-lowering* effect [34] has been neglected, because in metastability the voltage at the drain is around $V_{\text{DD}}/2$.

Combining (3)–(6) for N- and P-type transistors the following proportionality is derived:

$$\tau \propto \frac{T^{\alpha_\mu}}{(V_{\text{DD}} - (V_{\text{ThNo}} + \alpha_{VThN}(T - T_0) - |V_{\text{ThPo}} + \alpha_{VThp}(T - T_0)|))^{\alpha}}. \quad (7)$$

By using (7), we can derive the following semiempirical formula for (T, V_{DD}) dependence of τ:

$$\tau(T, V_{\text{DD}}) = \frac{A \cdot T^{\alpha_\mu}}{(V_{\text{DD}} - (2V_{\text{ThE}} + \alpha_{VThE}(T - T_0)))^{\alpha}} \quad (8)$$

where V_{ThE} is the effective threshold voltage, α_{VThE} is the effective voltage temperature coefficient, and A is the multiplicative constant with appropriate units.

B. T_W Model

In contrast with the model for τ, we use an empirical model for T_W with respect to (T, V_{DD}), because T_W does not constitute an inherent physical constant of the system. Rather, it is a coefficient arising from MTBF modeling [35]. We have chosen a relatively simple model based on trading off accuracy for simplicity, for two reasons. First, because the effect of T_W on MTBF is linear (1), its influence on MTBF is significantly smaller compared with the exponential effect of τ. Thus, reducing accuracy in the modeling of T_W will result in a relatively small inaccuracy in MTBF. Second, the model employs fitting to T_W values determined by simulations and measurements; these values are noisy, and a low-order fitting model is preferred as it avoids overfitting, effectively low-pass filtering the noise. We validate those assumptions in the following sections, where we present results, and compare values of MTBF by using different T_W bounds.

On the basis of measurements and simulations [4], a nonlinear model for T_W is proposed

$$T_W(T, V_{\text{DD}}) = \sum_{i,j=1}^{2} a_{i,j} x_i x_j + \sum_{i=1}^{2} b_i x_i + c \quad x_1 = T \quad x_2 = V_{\text{DD}}. \quad (9)$$

The coefficients $a_{i,j}$, b_i $(i, j, \epsilon\{1, 2\})$, and c are determined by a nonlinear least-square procedure. The constants $a_{1,2}$ and $a_{2,1}$ are both coefficients of square terms of the form TV_{DD} and are grouped in a single coefficient named $\tilde{a}_{1,2}$. Overall for the T_W model, we are left with six parameters: $a_{1,1}, a_{2,2}, \tilde{a}_{1,2}, b_1, b_2, c$.

C. MTBF Model

To express the MTBF dependence on T and V_{DD}, we combine (1), (8), and (9) to obtain

$$\text{MTBF}(T, V_{\text{DD}}) = \exp \frac{\left(\frac{S}{A \cdot T^{\alpha_\mu}(V_{\text{DD}} - (2V_{\text{ThE}} + \alpha_{VThE}(T - T_0)))^{-\alpha}}\right)}{\left(\sum_{i,j=1}^{2} a_{i,j} x_i x_j + \sum_{i=1}^{2} b_i x_i + C\right) \times F_C \times F_D}. \quad (10)$$

We define two useful parameters, the temperature coefficient of MTBF (TCM) and the supply voltage coefficient of MTBF (VCM). TCM expresses the relative change of MTBF when the temperature is changed by 1 K. The VCM is the

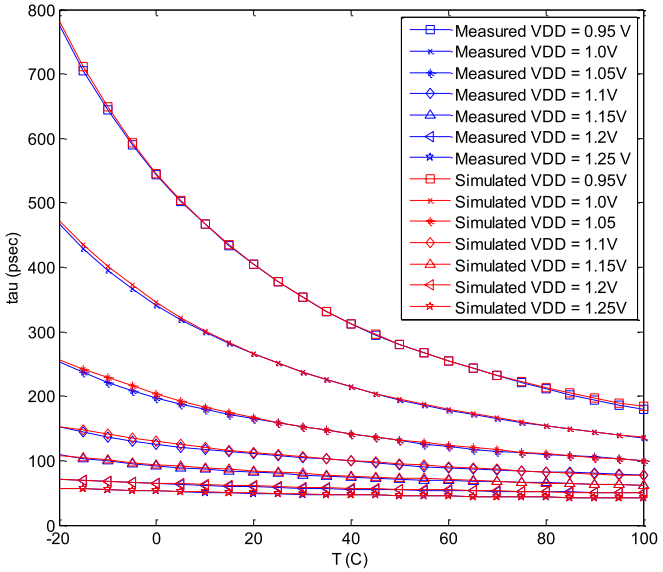

Fig. 3. τ measurements and simulation results versus temperature for different supply voltages.

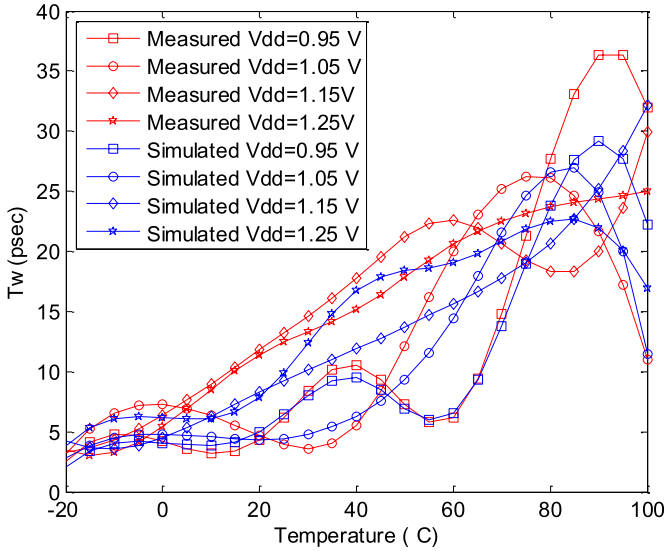

Fig. 4. τ measured and simulated results versus temperature for different supply voltages.

analogous form for supply voltage change of 1 V. TCM and VCM estimations can be obtained from (10)

$$\text{TCM} \triangleq \frac{1}{\text{MTBF}}\frac{\text{dMTBF}}{dT} = -\frac{S}{\tau}\left(\frac{1}{\tau}\frac{d\tau}{dT}\right) - \left(\frac{1}{T_W}\frac{dT_W}{dT}\right). \quad (11)$$

In a similar way

$$\text{VCM} \triangleq \frac{1}{\text{MTBF}}\frac{\text{dMTBF}}{dT_{\text{DD}}} = -\frac{S}{\tau}\left(\frac{1}{\tau}\frac{d\tau}{dV_{\text{DD}}}\right) - \left(\frac{1}{T_W}\frac{dT_W}{dV_{\text{DD}}}\right). \quad (12)$$

The expressions in parentheses in (11) and (12) are the relative change in τ multiplied by the factor s/τ, and the relative change in T_W when T or V_{DD} are increased by 1 K or by 1 V, respectively.

IV. Model Evaluation

To evaluate the validity of the proposed model, we compare it with measurments and simulations (which were described in [4]). A synopsis of measurements and simulation results are given, followed by comparing them with model results, and by analyzing the MTBF sensitivity by means of TCM and VCM parameters.

A. Simulations and Measurements Results

Fig. 3 shows a comparison of τ simulations and measurements for a 65 nm LP CMOS library master–slave flip-flop (Fig. 2) used as a synchronizer. The measurements have been performed in preselected typical/typical (TT) parts, which correspond to typical process corners of the fabrication process both for N and P transistors. The results represent an average of eight measured chips, and the empirical standard deviation of the measurements is less than 5% for each supply voltage value. Simulations used for comparison were carried out using the method described in [36] and [37], which sweeps clock and data signals to predict τ and T_W values.

The difference between τ measurements and simulations is less than 3.2% under the entire set of supply voltages and temperature combinations. As described in [4], this difference is consistent with the measurement error in τ, estimated at 5%.

Fig. 4 shows T_W measured and simulated results versus temperature for different supply voltages. Simulated values show an oscillatory trend due to simulation dependence upon initial conditions and integration error. Measured values of T_W are highly affected by absolute errors in the delay measurements [4]. Owing to high process variations in deep submicrometer technologies, the delay for some gates can differ greatly from the mean delay of identical gates in the circuit. Those variations may reach 40% in 65 nm [38], and affect T_W measurements as shown in [4]. In Section V, we evaluate the error incurred using different T_W bounds, and their impact on MTBF.

B. Model Results

In this section, we compare the model derived in Section III to measured and simulated values, and calculate the accuracy of the model for different technologies.

Fig. 5 shows a comparison of model (8) (solid surface) and measured values for τ (dots). Figs. 6 and 7 show voltage and temperature cross sections of Fig. 5. The empirical model parameters were obtained by means of a trust-region nonlinear least-square approximation [39], [40] of the measured values with respect to (8), as shown in Table II. The method used for the fit is a Levenberg–Marquardt algorithm [41], that can be viewed as an extension of the Gauss method to find the roots of a function. In addition, we constrain the possible values of the model parameters to physical feasibly values. The goodness of fit is given by the coefficient of determination (R-square) and the adjusted R-square. Both are needed to avoid a scenario of *Anscombe's quartet* [42], where an R-square value close to unity does not guarantee a good fit because of model over fitting. In our case, both R-square

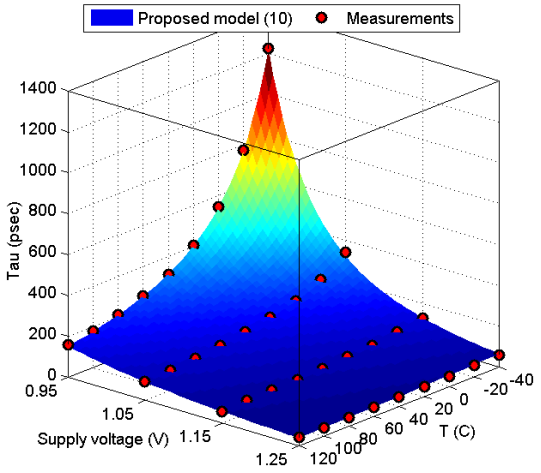

Fig. 5. τ analytic model versus measurements results.

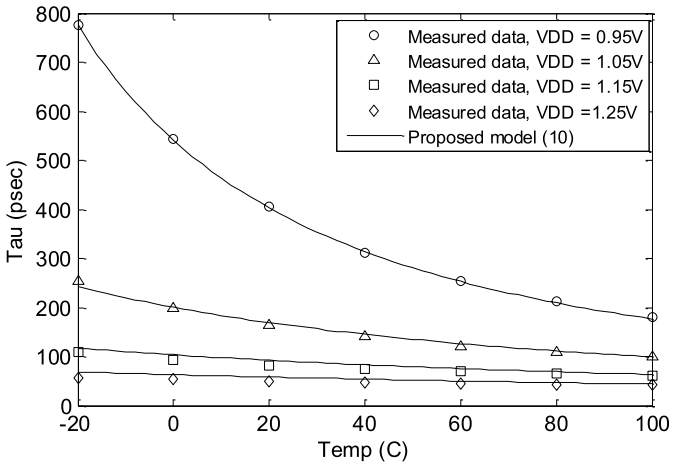

Fig. 6. Measurements versus analytical model, temperature cross sections of Fig. 5.

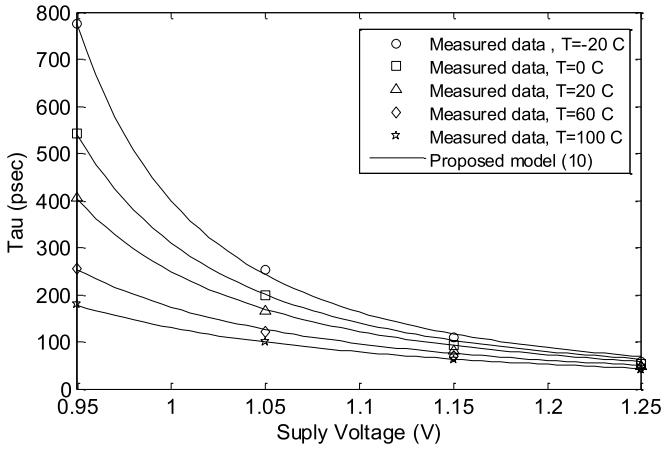

Fig. 7. Measurements versus analytical model, supply voltage, cross sections of Fig. 5.

and the adjusted R-square values are close to unity, indicating a good fit of the model to measurements. In addition, Figs. 6 and 7 show that there are no outliers in the data set. The root mean square error (RMSE) of the fit determines that the average error induced in using the model compared with

TABLE II
NONLINEAR LEAST-SQUARE FIT OF τ MEASUREMENTS

PARAMETERS	VALUE	UNITS
A	0.00068	
α_μ	1.7	
$2V_{ThE}$	0.784	[V]
α_{VThE}	-1.9	[mV/K]
α	2.8	
T_0	233	[K]
RMSE	2.93	ps
R -square	0.9996	
Adjusted *R -square*	0.9993	

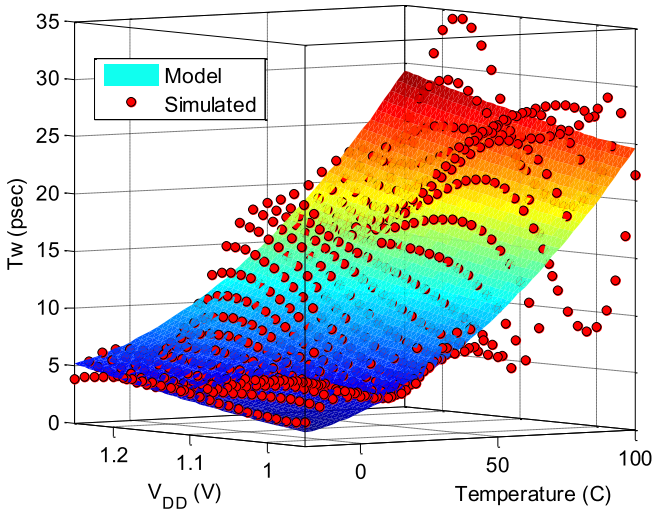

Fig. 8. T_W model versus simulated values.

measurements is under 2% in average. Because measurements were shown to follow simulations within less than 5% error (in Section IV-A), simulations can be used with confidence to determine model parameters as well. When the supply voltage is high, the temperature influence on τ is reduced (bottom of Fig. 6), but for lower supply voltage values, a change in temperature may lead to large changes in τ (top of Fig. 6). Supply voltage though, increases τ significantly for every temperature in the range -20 °C to 100 °C, the influence becomes larger when the temperature is low (Fig. 7).

In general, at least five sets of readings $\{(T_i, V_{\mathrm{DD}i}, \tau_i)\}_{i=1,\ldots,5}$ are needed to estimate the five model parameters $(A, \alpha, \alpha_{VThE}, \alpha_\mu, V_{\mathrm{ThE}})$. Those sets are likely to be obtained by simulations or measurements.

Fig. 8 shows a comparison of T_W model (9) and simulations. In this case, the model represents the trend of T_W for different (T, V_{DD}) as the simulated (or measured) data are noisy. Modeling T_W as a higher order polynomial would produce overfitting to noise data and will not generate reliable values. Table III shows the estimated coefficients of the nonlinear least-square fit of the simulated T_W to (9). The R-square indicator is significantly lower than 1 (around 0.85); however, this ends up in only a small deviation of the MTBF as is

TABLE III
NONLINEAR LEAST-SQUARE FIT OF T_W SIMULATIONS

PARAMETERS	VALUE	UNITS
$a_{2,2}$	0.0954	ps V^{-2} [a]
$\tilde{a}_{1,2}$	0.0762	ps K^{-1} V^{-1} [a]
$a_{1,1}$	1.541	ps K^{-2} [a]
b_1	7.146	ps K^{-1}
b_2	1.33	ps V^{-1}
c	-11.96	ps
RMSE	3.17	ps
R -square	0.8455	
Adjusted R -square	0.8442	

[a]V = volt, K=degree kelvin.

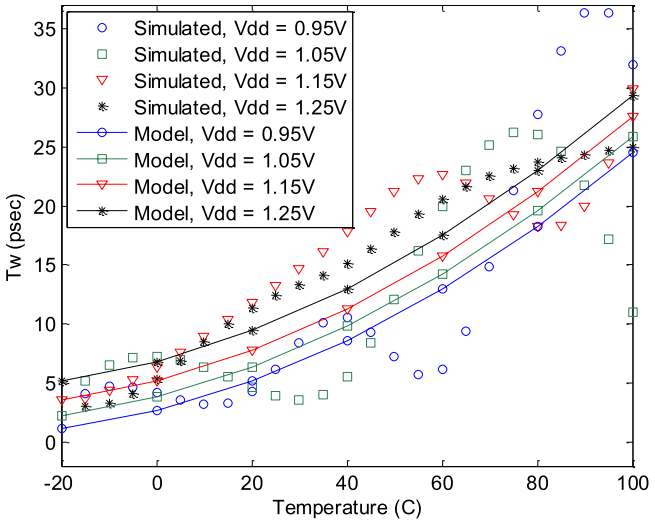

Fig. 9. Simulations versus analytical model, temperature cross section shown in Fig. 8.

demonstrated in the following section. Values of the RMSE demonstrate that the average deviation remains small compared with absolute T_W values. Temperature cross sections of the T_W model for different supply voltages are shown in Fig. 9.

T_W increases with temperature approximating a quadratic function. The parabolic nature of T_W is almost unchanged for different supply voltages, as shown by the near parallel curves in Fig. 9. T_W also shows an increase with supply voltage, although that change is much smaller than the change with temperature.

Fig. 12 shows MTBF model (10) versus simulations. The MTBF corresponds to a clock domain crossing of $f_d = 100$ MHz and $f_c = 500$ MHz, using a two flip-flop synchronizer. A black plane representing MTBF threshold is also shown, set to 25 years as a representative number. All points with MTBF above the threshold are reliable; points below the threshold are considered unreliable and a circuit operating at that (T, V_{DD}) point is prone to metastability failures. The green surface is the MTBF value calculated using the model and the violet surface is MTBF calculated using

TABLE IV
NONLINEAR LEAST-SQUARE FIT RESULTS FOR DIFFERENT TECHNOLOGY NODES

PROCESS NODE	τ		T_W	
	R- SQUARED	ADJUSTED R-SQUARED	R- SQUARED	ADJUSTED R-SQUARED
180nm[b]	0.999	0.998	0.8113	0.8091
90nm[b]	0.9991	0.998	0.832	0.8319
65nm[a]	0.9996	0.9993	0.8455	0.8442
45nm[b]	0.991	0.983	0.877	0.891
32nm[b]	0.997	0.992	0.813	0.809

[a]Low power (LP), [b]General purpose (GP)

simulated values of τ and T_W. The main difference between the surfaces is due to the difference between the T_W model and simulations (rather than to any differences in τ).

Fig. 10(a) shows τ temperature sensitivity $[(1/\tau)(d\tau/dT)]$ for different supply voltages. When the supply voltage is higher than the nominal voltage of the technology (1.1 V for low power 65 nm) τ changes moderately. However, for lower V_{DD} a small temperature change leads to a large percentage change in τ. For $V_{\mathrm{DD}} = 0.95$ V, $T = 40$ °C an increase of 1 K results in a 1.2% decrease in τ. In the temperature region, we studied (−20 °C to 100 °C) both μ and V_{Th} decrease with increasing temperature [43]; however, decreasing μ increases τ while decreasing V_{Th} decreases τ. When the impact of a change in μ on τ is larger than the impact of a change in V_{Th} on τ, increasing temperature causes an increase in τ. Conversely, when the impact of V_{Th} dominates over that of μ, increasing temperature causes a decrease in τ. The dominant factor is determined by the value of the supply voltage. In modern technologies, where V_{DD} approaches the value of $2V_{\mathrm{Th}}$, small changes in V_{Th} cause larger changes in τ, and it is dominant over μ.

In addition to showing good match of measurements, simulations and model results on 65 nm LP process, the model was tested against τ, T_W simulations for 180 and 90 nm and 45 and 32 nm technology nodes. All the results present higher than 0.99 values for R-square and adjusted R-square fit for τ to (8), and higher than 0.85 fit for T_W to (9) as shown in Table IV.

Fig. 10(b) shows τ supply voltage sensitivity $[(1/\tau)(d\tau/dV_{\mathrm{DD}})]$ for different temperatures. For high temperatures, V_{Th} decreases and the influence of V_{DD} on τ is smaller. For lower temperatures, V_{Th} is larger and when V_{DD} is decreased τ increases by larger margins. In both cases, τ sensitivity to V_{DD} and T, the dependence is negative, that is, an increase in V_{DD} or T will induce a decrease in τ. Such analysis is useful, for instance, to specifying the stability of power supplies and power distribution networks on chip. When the amount of noise in the power supply is known, the effect induces a change in τ and a possible decrease in system metastability reliability. This is more significant when voltage drops are present (IR-drops), reducing the effective supply voltage seen by the synchronizer circuit and hence increasing τ, which according to (12) reduces MTBF.

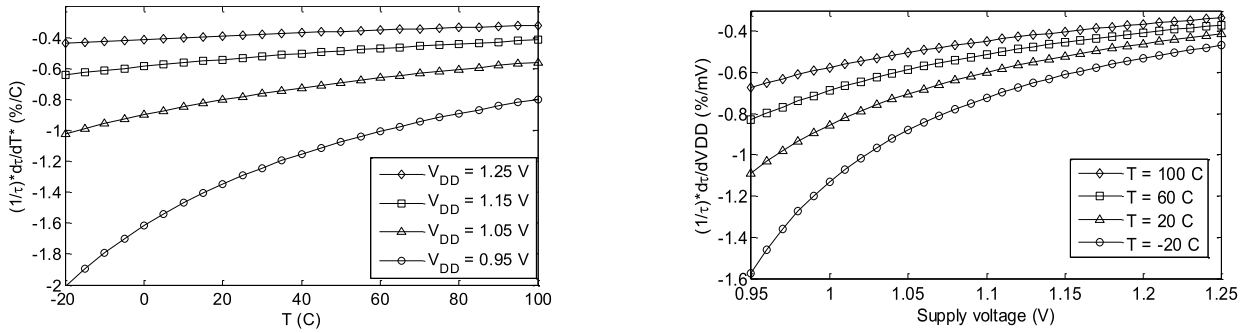

Fig. 10. (a) τ temperature sensitivity $[(1/\tau)(d\tau/dT)]$. (b) τ supply voltage sensitivity $[(1/\tau)(d\tau/dV_{\mathrm{DD}})]$.

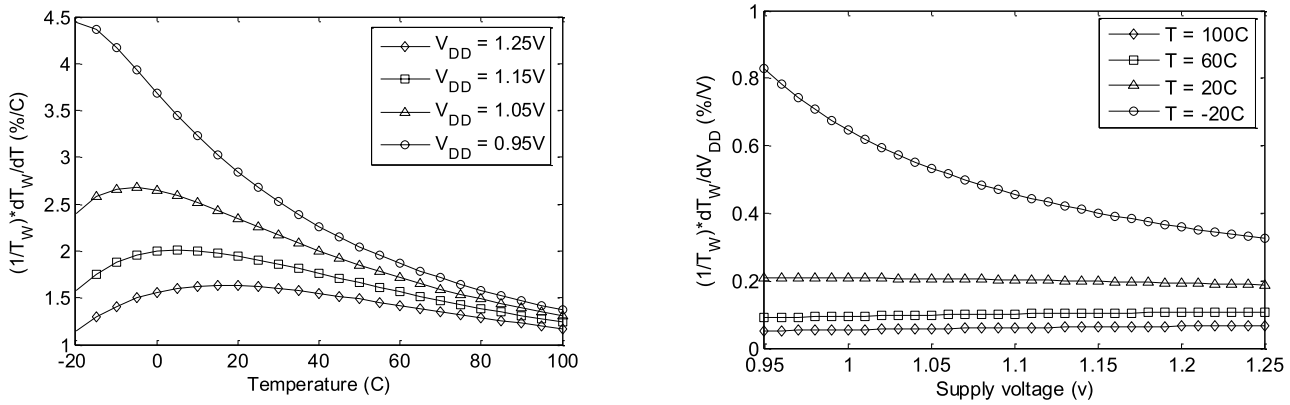

Fig. 11. (a) T_W temperature sensitivity $[(1/T_W)(dT_W/dT)]$. (b) T_W supply voltage sensitivity $[(1/T_W)(dT_W/dV_{\mathrm{DD}})]$.

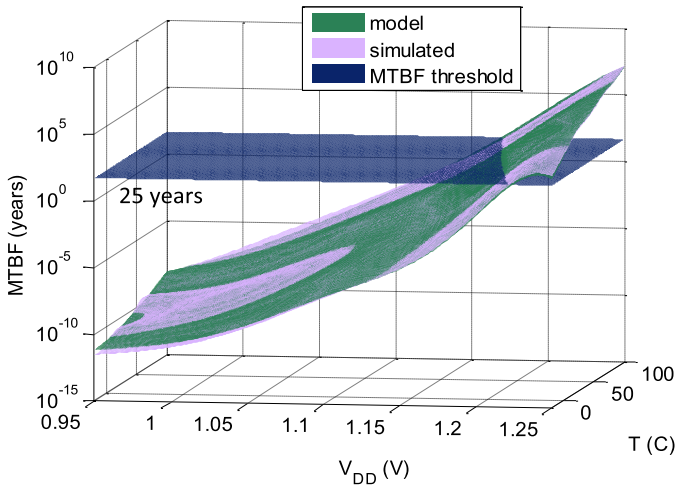

Fig. 12. MTBF model versus simulated results.

Analogously, Fig. 11(a) shows temperature sensitivity $[(1/T_W)(dT_W/dT)]$ of T_W for different supply voltages. Sensitivity increases for lower supply voltages. In Fig. 11(b), supply voltage sensitivity $[(1/T_W)(dT_W/dV_{\mathrm{DD}})]$ of T_W is shown. For nominal and high temperatures, the sensitivity is almost constant and around 0.2%/V. For lower temperatures, the sensitivity increases but still remains lower than 1%/V. Consequently, T_W is less sensitive to supply voltage variations than to temperature variations.

C. TCM and VCM Results

Fig. 13 shows TCM curves versus temperature for $V_{\mathrm{DD}} = 1.1$ V. The graph shows the different components of TCM as in (11). The resolution time (S), is given by $S = NT_C - t_{\mathrm{SU}}(\mathrm{FF}) - t_{\mathrm{ic}}$, where $t_{\mathrm{SU}}(\mathrm{FF})$ is the setup time of the receiving flip-flop after the synchronizer, and t_{ic} is the parasitic interconnect delay between the flip-flops (usually minimal as they are placed close together). For a given design, S varies with $(T,\ V_{\mathrm{DD}})$ due to $t_{\mathrm{SU}}(\mathrm{FF})$ and t_{ic} variations. However, by changing the design value of T_C, it may be possible to maintain $S = 10\tau$ even when $(T,\ V_{\mathrm{DD}})$ vary. Consider these two cases, as follows. First, assume that T_C is held constant, in spite of varying $(T,\ V_{\mathrm{DD}})$. $S(T,\ V_{\mathrm{DD}})$ decreases when V_{DD} decreases because the parasitic delays $[t_{\mathrm{pd}}(\mathrm{FF}),\ t_{\mathrm{SU}}(\mathrm{FF}),\ t_{\mathrm{ic}}]$ increase. As τ increases when V_{DD} is decreased, the S/τ factor in (11) and (12) is decreased. Second, if T_C is modified when $(T,\ V_{\mathrm{DD}})$ change, as is often the case in real circuits, the factor S/τ should be evaluated as a function of $(T,\ V_{\mathrm{DD}})$ and of the change in T_C, and in certain situations it may be possible to maintain $S = 10\tau$.

In the following examples and for ease of calculation, it is assumed that the receiver clock domain period (T_C) is modified when $(T,\ V_{\mathrm{DD}})$ changes to maintain $S = 10 \cdot \tau(T,\ V_{\mathrm{DD}})$. The trend of TCM is mainly affected by the τ sensitivity and is slightly reduced by the T_W sensitivity. For instance, when the circuit operates at room temperature (27 °C), an increase of one degree in temperature generates a reduction of 8.1%

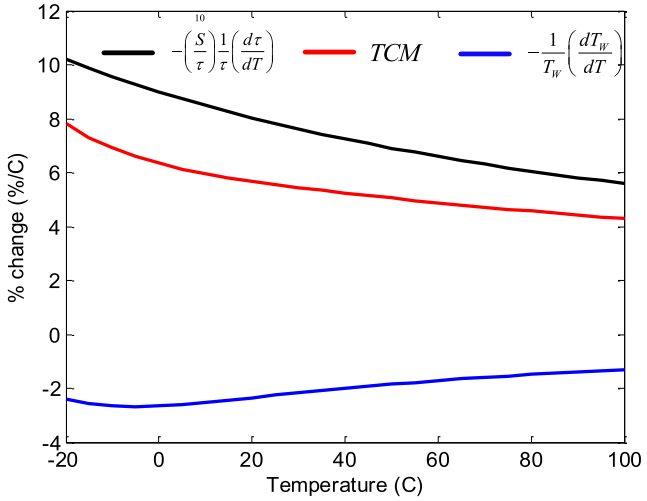

Fig. 13. TCM versus temperature ($V_{DD} = 1.1$ V).

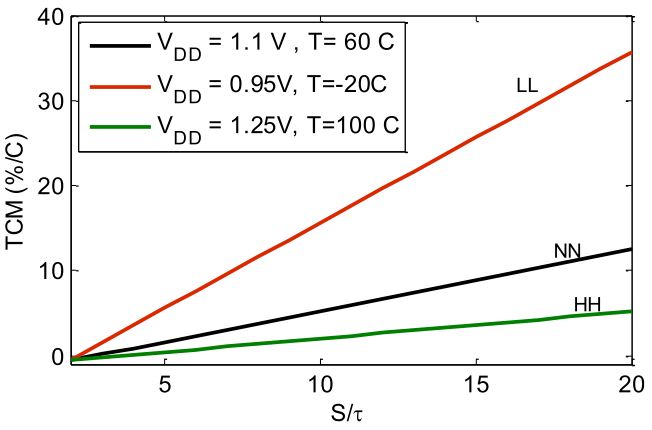

Fig. 14. TCM versus resolution time for different (T, V_{DD}) corners.

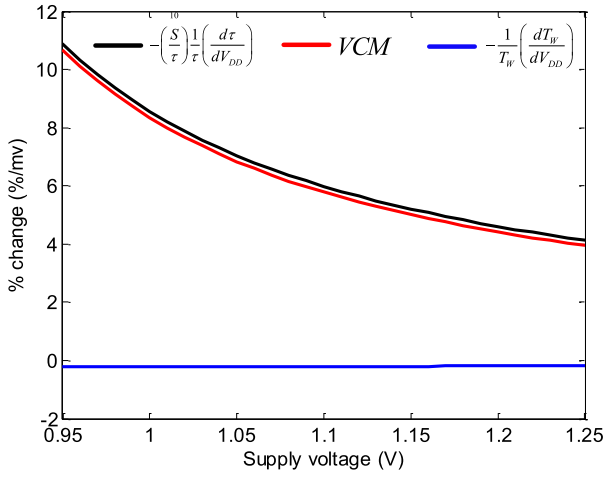

Fig. 15. VCM versus temperature ($\tau = 40$ °C).

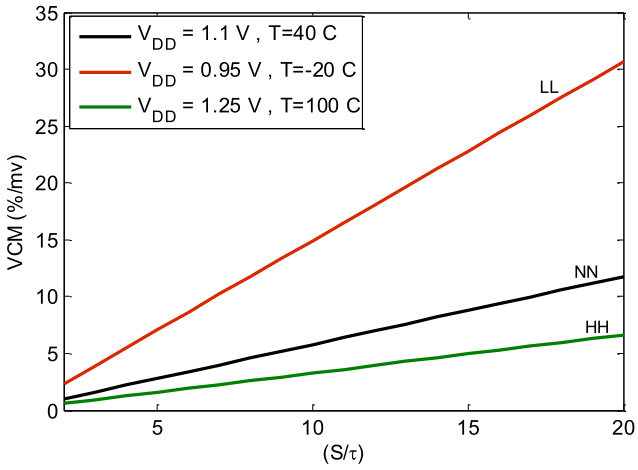

Fig. 16. VCM versus resolution time for different (T, V_{DD}) corners.

in the first term of (11), an increase of almost 1.8% in the second term, and an overall 6.3% increase in MTBF (assuming $S = 10\tau$).

The absolute percentage change in MTBF is determined by the (T, V_{DD}) operating point, and by S, the amount of resolution time. Fig. 14 shows TCM versus normalized resolution time for three different corners: low supply voltage, low temperature corner (LL), nominal voltage, nominal temperature (NN), and high voltage, high temperature (HH). In all cases, TCM increases as resolution time increases, following the linear equation described in (11). When the system is operated near the LL corner, small S changes generate higher percentage MTBF fluctuations.

It should be noted, that the corner case LL corresponds to a low voltage, *low* temperature case as opposed to delay corners when the slowest circuits appear for low voltage and *high* temperature. In a similar way, the HH case correspond to a high voltage, *high* temperature, and for delay, it is obtained for high voltage and *low* temperature.

Analogous plots for VCM are shown in Figs. 15 and 16.

The TCM and VCM tools used through this analysis are useful to determine the sensitivity of MTBF for different (T, V_{DD}) operating points. This is especially useful practically when evaluating the MTBF robustness to noise in the power distribution network, or fluctuations on temperature.

V. Model Implications

In this section, we study the effect of using different bounds for T_W and their impact on the MTBF. We also analyze the effects of using those bounds from the perspective of the VLSI designer who is to calculate the number of flip-flops to use in a synchronizer. We finish by presenting useful guidelines to the designer to account for corner (T, V_{DD}) conditions.

A. T_W Bounds

So far, we have developed a model for MBTF according to the models for τ and T_W. The τ model was shown to predict simulation and measurement values with minimal error, but T_W model demonstrates a higher error due to the noisy nature of measurements and simulations that were used to fit into the model. In this section, we analyze the effect that the

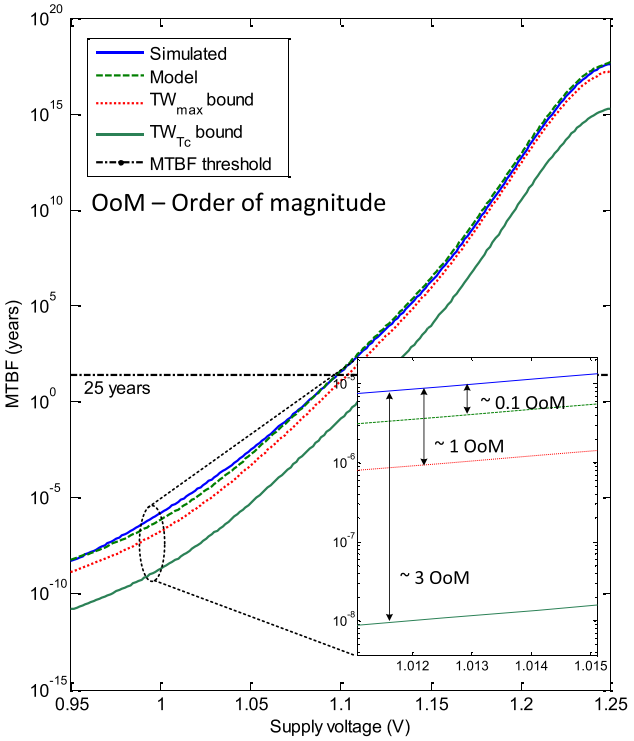

Fig. 17. MTBF versus supply voltage for $f_d = 100$ MHz, $f_c = 300$ MHz, using simulations, model and bounds for T_W.

T_W model has on MBTF and the number of flip-flops to use in a synchronizer. We study different bounds that compromise accuracy for simplicity.

We compare simulated MBTF values, model calculated values (10), and two bounds named $T_{W\max}$ and T_{WTc}. $T_{W\max}$ is the maximum T_W over all (T, $V_{\rm DD}$) combinations, and T_{WTc} is the clock period, as clearly $T_W \leq 1/f_c = T_C$.

Fig. 17 shows MTBF results of simulations, model, and $T_{W\max}$ and T_{WTc} bounds for a system with $f_d = 100$ MHz, $f_c = 300$ MHz by using a two flip-flop synchronizer. We note that the simulated and model results are correlated with a maximum difference of less than 30%, much less than an order of magnitude for the entire range of supply voltage studied. $T_{W\max}$ represents a lower bound with a maximum difference of one order of magnitude related to simulated MTBF values. The T_{WTc} bound provides a less tight lower bound with difference of almost three orders of magnitude below model predictions. The MTBF difference for each of the bounds can be translated to the number of flip-flops to use in a synchronizer to obtain a target MTBF of 25 years. Fig. 18 shows the number of flip-flop stages to use when $f_d = 100$ MHz, $f_c = 300$ MHz, and $T = 27$ °C. For the nominal supply voltage (1.1 V), model and simulations indicate that a two flip-flop synchronizer should be used. However, the T_{WTc} bound indicates a three flip-flop synchronizer incurring an extra delay of one clock cycle. The difference of the number of stages calculated using the different bounds represents the overprovisioning of each bound. It is clearly noted that the minimum overprovisioning is obtained by the developed model, which for lower supply voltages almost overlaps simulations.

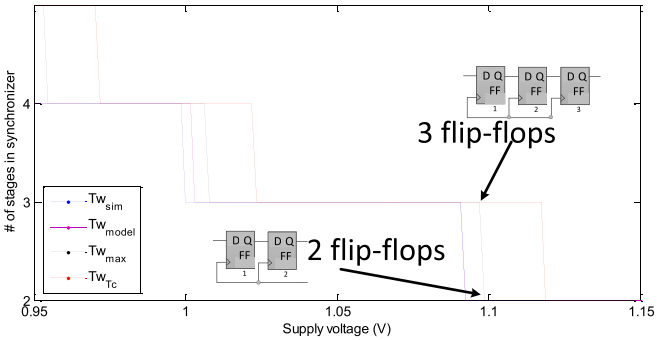

Fig. 18. Number of stages in synchronizer versus supply voltage, using different T_W bounds.

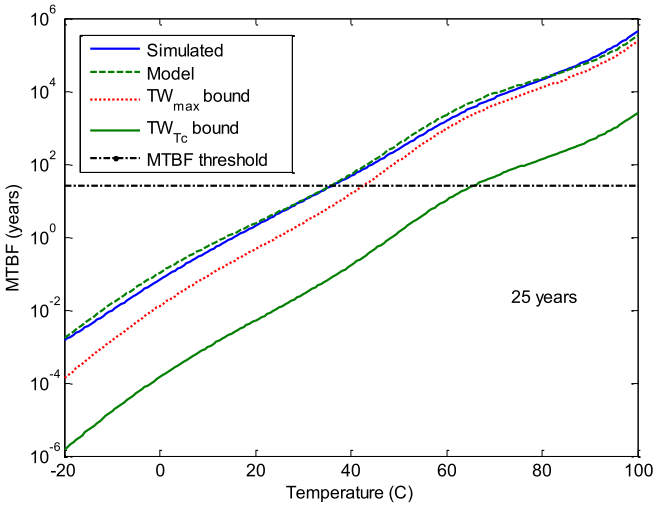

Fig. 19. MTBF versus temperature for a $f_d = 100$ MHz, $f_c = 300$ MHz, using different T_W bounds.

Fig. 19 shows results of MTBF versus temperature for the same system as above. The model derived is still closely related to simulations with differences of less than 30% over the studied temperature range, but the bounds present much larger deviations from both simulations and model of one and three orders of magnitude, respectively. It is worth noting that both bounds present higher differences for lower temperatures and supply voltages, which as noted above are the worst cases with respect to metastability resolution.

B. Synchronizer Design Considerations

In this section, we study the model implications from the perspective of the VLSI designer who needs to determine the number of stages to use in a synchronizer, according to the system parameters, the sender and receiver frequencies (f_d, f_c), the technology node and flip-flop libraries which determine τ and T_W, and the reliability of the intended system, as measured by MTBF. The usual approach to this task is to estimate the amount of resolution time needed to obtain a certain MTBF by using (1), followed by the calculation of the number of flip-flop stages to achieve that resolution time. Usually a spare number is always added to account

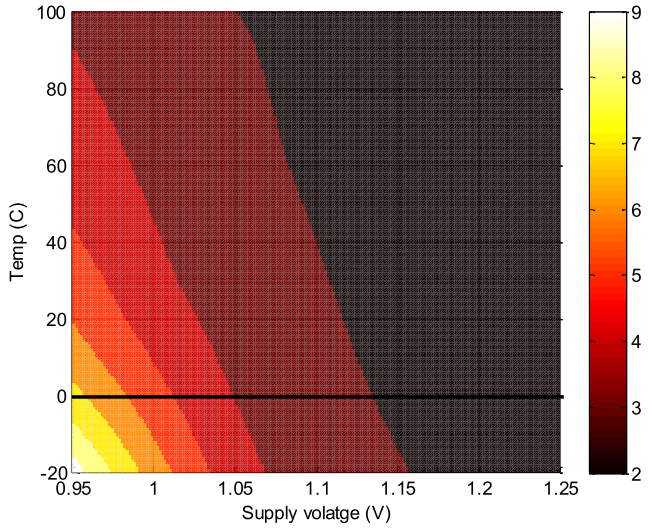

Fig. 20. Number of flip-flops in synchronizer for $F_C = 30$ MHz and $F_D = 100$ MHz.

for variations. This spare number can be added to the target MTBF or to the calculated number of stages, but is usually determined by rules of thumb, rather than by quantitative calculations, possibly yielding loose bounds with significant performance loss or underestimations resulting in metastability errors. In this section, we identify design guidelines that provide tighter bounds to MTBF and hence alleviate the need of unnecessary flip-flop stages.

To understand the implications of the measurements and model results, we consider synchronization scenarios and calculate the number of stages to be used to achieve a desired reliability. This calculation is based on the model (10), the desired MTBF and the assumption that each additional stage adds a clock period to the settling time S in (1), as proposed in [35]. Model parameters are obtained from previous measurements of a 65 nm LP process and standard digital library flip-flops (Tables II and III). It is also assumed that both master and slave latches in the prospective flip-flops have the same τ and T_W, a usually optimistic assumption [28], but is assumed here for the ease of calculation. We also omit the setup time and propagation delay of each flip-flop.

The first guideline is the need to account for the worst case scenario. As was stated in the previous section (Figs. 14 and 16) the worst synchronization scenario occurs at the low temperature, low supply voltage corner. Fig. 20 shows the number of flip-flop stages needed in a synchronizer to achieve an MTBF of 25 years, for a system with $f_d = 100$ MHz, $f_c = 300$ MHz. The number of flip-flops increases drastically for the worst case corner, incurring a very high latency. It is possible to assume that when a circuit is in functional operation, the self-heat generated raises the junction temperature of internal nodes in the circuits above 0 °C; thus, the black line in Fig. 20 shows a zero-degree junction temperature limit, below which actual practical operation is unlikely to be encountered. Even when this zero-degree junction temperature limit is considered, the number of flip-flops in nominal operation mode is very different than in the worst case.

A typical error is to omit the worst (T, VDD) corner analysis, and substitute it by an increased MTBF target to account for T, $V_{\rm DD}$ variations. In other words, calculate the number of stages for the nominal (T, $V_{\rm DD}$) corner by using an increased MTBF target value (i.e., doubled MTBF) to account for the (T, $V_{\rm DD}$) variations.

The number of stages (N_S) for a given synchronization is given by (1)

$$N_S \left\lceil \frac{\tau \cdot \ln(\text{MBTF} \cdot F_c \cdot F_d \cdot T_W)}{T_C} \right\rceil + 1. \tag{13}$$

The main difference between the nominal (T, $V_{\rm DD}$) case and the worst case is reflected by different τ and T_W as shown in Figs. 5 and 8. Because τ dominates (Figs. 13 and 15), it is the dominant factor in the worst case, where the number of stages is given by

$$N_S^{wc(T,V_{\rm DD})} \cong N_S^{\rm nom} \left(\frac{\Delta\tau}{\tau} + 1 \right) \tag{14}$$

where $\Delta\tau$ is the increase in τ for the worst case corner. In the 65 nm example, $\Delta\tau/\tau \approx 3$ for the worst case and $N_S^{wc(T,V_{\rm DD})} \approx 4\, N_S^{\rm nom}$. If for the nominal ($T$, $V_{\rm DD}$) corner, only two synchronization stages are needed to obtain a desired MTBF, then in the worst case scenario, the number of flip-flops increases to around 8.

On the other hand, the number of stages needed when an MTBF spare (ΔMTBF) is taken, is given approximately by

$$N_S^{\rm MTBF+\Delta MTBF} \cong N_S^{\rm MTBF} + \left\lceil \frac{\tau}{T_C} \frac{\Delta\text{MTBF}}{\text{MTBF}} \right\rceil. \tag{15}$$

Typically a spare of 50%–100% is taken, giving values of (ΔMTBF/MTBF) ≈ 1. As $\tau < T_C$, this implies that either $N_S^{\rm MTBF+\Delta MTBF} \cong N_S^{\rm MTBF}$ or $N_S^{\rm MTBF+\Delta MTBF} \cong N_S^{\rm MTBF} + 1$. This means that doubling the MTBF target adds only one stage to the synchronizer at most. Contrast this result with the need to multiply the number of stages by 4, discussed previously.

Designing for worst case, as suggested in this section, may result in extremely high latency, which may be prohibitive in some applications. As is evident from the previous examples, synchronization parameters are functions of supply voltage and temperature. These parameters tend to change dynamically during functional operation. Because a large number of flip-flops is needed only in corner cases, it is possible to dynamically adapt the number of synchronization stages according to τ measurements (as presented, for instance, in [4]). With such an adaptation, a tradeoff between latency and reliability can be achieved for typical scenarios without compromising reliability in corner cases.

VI. Conclusion

We presented a model that is able to predict MTBF for different levels of supply voltage and temperature. The model is based on a semiempirical model developed for the resolution time constant τ and on an empirical model for the metastability window T_W. The τ model was shown to be highly accurate with respect to measurements and simulations, with errors

below 2%. The model is based on five semiempirical parameters (A, α, α_{VThE}, α_{μ}, and V_{ThE}) which are obtained from curve fitting to simulated or measured data. The T_W model is based on six empirical parameters ($a_{1,1}$, $a_{2,2}$, $\bar{a}_{1,2}$, b_1, b_2, and c), which are obtained by a nonlinear least-square regression to simulated or measured values.

Models for τ, T_W, and MTBF were shown to provide accurate prediction of values relieving the need for simulations or measurements for different (T, V_{DD}) corners.

The concepts of TCM and VCM were introduced, which are useful to understand the sensitivity of MTBF with respect to changes in τ and T_W. Both VCM and TCM were studied. MTBF was shown to present worst case scenarios under low temperature and low supply voltage conditions, where the sensitivities to variations peaked.

Bounds for T_W were studied and their influence on MTBF was evaluated. Both $T_{W\max}$ and T_{WTc} bounds were shown to provide less tight lower bounds on MTBF. Moreover, we showed that using the bounds to calculate the number of stages of a synchronizer may result in unnecessary large margins in the number of flip-flops to use compared with model calculations. The model presented was shown to predict the number of flip-flops in good correlation with simulations.

With the derived model, we proposed synchronizer design guidelines to account for temperature and supply voltage variations.

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